



PHD DISSERTATION



***On the Effect of Surface Texture
and Nanoscale Surface Oxides on
the Optical and Mechanical
Properties of Silicon Single Crystals
and MEMS Thin films***

November 2015

**Fashina Adebayo Adebeye
(70078)**

**DEPARTMENT OF THEORETICAL AND APPLIED PHYSICS,
AFRICAN UNIVERSITY OF SCIENCE AND TECHNOLOGY,
ABUJA, NIGERIA**



***On the Effect of Surface Texture and Nanoscale
Surface Oxides on the Optical and Mechanical
Properties of Silicon Single Crystals and MEMS
Thin Films***



Fashina Adebayo Adeboye
(70078)

**A Dissertation Submitted to the Department of Theoretical and Applied
Physics in Partial Fulfillment of the Requirements for the Degree of**

Doctor of Philosophy

at the

African University of Science and Technology, Abuja

PhD Dissertation Committee:

Professor W. O. Soboyejo, (Princeton University, USA), Chair

Associate Professor M. G. Zebaze Kana (KWASU, Nigeria)

Associate Professor Omololu Akin-Ojo (AUST, Nigeria)

Professor Oleg Yordanov (Bulgarian Academy of Sciences, Bulgaria)

November 2015

PREFACE

This dissertation presents a recent work carried out between February 2012 and May 2015 at the African University of Science and Technology, Abuja, the Sheda Science and Technology Complex (SHESTCO), Abuja and the Princeton Institute of Science and Technology of Materials (PRISM), Princeton University, NJ, USA under the supervision of Professor Winston Oluwole Soboyejo and Dr. M. G. Zebaze Kana. This write up is divided into six chapters. These includes: the introductory chapter, literature review chapter, the chapter on analytical modelling, the chapter on experimental work, the chapter on computational modelling and the concluding chapter. This research work was financially supported by the World Bank STEP-B Program, the World Bank African Centers of Excellence Program, the African Development Bank (ADB), the African Capacity Building Foundation (ACBF) and the Nelson Mandela Institute (NMI).

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CERTIFICATION

**ON THE EFFECT OF SURFACE TEXTURE AND NANOSCALE SURFACE
OXIDES ON THE OPTICAL AND MECHANICAL PROPERTIES OF SILICON
SINGLE CRYSTALS AND MEMS THIN FILMS**

By

Fashina Adebayo Adebayo

A DISSERTATION APPROVED BY THE THEORETICAL AND APPLIED PHYSICS
DEPARTMENT

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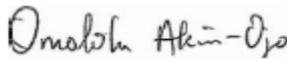
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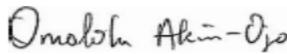
.....
Co-supervisor, Dr. M. G. Zebaze Kana



.....
Professor Oleg Yordanov



.....
Dr. Omololu Akin-Ojo



.....
Head, Department of Theoretical and Applied Physics

APPROVED:

.....
Vice President, Academics

Date:

DEDICATION

THIS RESEARCH WORK IS DEDICATED TO:

GOD ALMIGHT, WHO ALONE DOETH WONDEROUS THINGS, AND FOR HIS
UNMERITED LOVE, EXCEEDING GRACE, MERCIES AND DIVINE PROTECTION
ALL THROUGH MY GRADUATE STUDIES

MY BELOVED FAMILY, WHO'S CONTINUED SUPPORT, ENCOURAGEMENT AND
PERSISTENCE, HAS ENABLED ME TODAY TO BE IN THIS POSITION.

THANK YOU.

MY TRUE FRIENDS, WHO'S CONSTRUCTIVE CRITICISM HAS MADE ME A

BETTER MAN

THANK YOU.

ABSTRACT

This dissertation presents the combined results of analytical, computational and experimental study of the effects of surface texture and nanoscale surface oxides on the optical and mechanical properties of silicon single crystals and MEMS thin films. The first part of this work is focused on the analytical modeling of the reflectance of flat and textured silicon substrates. The model was used to study the reflection behavior of textured silicon surfaces under non-normal incidence. By characterizing the incident light and facets of the silicon wafer with vector geometry, dot products and Phong's reflection model were used to determine the reflection angles between incident light rays and pyramidal facets. The possible optical interactions are considered for a wide range of pyramidal geometries and light incidence angles that are relevant to the exposure of textured silicon surfaces to incident sunlight. Furthermore, the model was used to investigate the possibility of secondary reflection, for the full range of incidence angles to the substrate. The textured silicon surfaces were found to reduce the reflection angles more effectively than flat substrates at lower angles of incidence. Secondary reflection was also found to be experienced or guaranteed, for all pyramid heights, when the angle of incidence to the substrate was less than 19.4° . The predictions are validated with experimental measurements of reflectance from (001)-textured silicon surfaces. Secondly, the results of an experimental study of the effects of surface texture on the optical and light trapping properties of silicon wafers are presented. Surface texture is controlled by anisotropy etching with potassium hydroxide (KOH) and isopropyl alcohol (IPA) solutions. The effects of KOH/IPA etching on the uniform distribution of pyramidal textures on the (001)-oriented silicon wafer are elucidated. The effects of etchant concentration and KOH/IPA ratio are also explored, along with the effects of etching duration and temperature. The resulting surface morphologies are then characterized with atomic force microscopy and scanning electron microscopy. The optical reflectance associated with the

different surface textures are also determined using surface profilometry and Ultra-Violet (UV)-visible spectroscopy. The results show that IPA concentration has the strongest effect on the surface roughness of (001)-single crystal crystals at temperatures up to 80°C. Above this value, evidence of temperature-induced cracking was revealed on the silicon substrate. The best volume concentration ratio of KOH: IPA is also found to be 2:4. In an effort to ascertain the effectiveness of the texturing process for light trapping scheme, simple 1 x 1 cm² solar cell devices with the structure of ITO/p-Si/Al were fabricated on both textured and flat silicon wafers. Finally, analytical and computational models for the study of fatigue crack nucleation in silicon micro-electro-mechanical systems (MEMS) structures are presented. Finite element modeling is used to study the role of stress-assisted dissolution on the formation and growth of cracks in the topical SiO₂ layer on the silicon MEMS structures. The possible formation and growth of cracks by such dissolution is elucidated and compared with measured surface profiles from prior work using Atomic Force Microscopy (AFM). The experimental results are also compared with predictions from linear perturbation analysis of the stability of surface topology that evolves during stress-assisted dissolution of the silica layer. The implications of the results are then discussed for the development of micro-pyramids for light trapping and improved photo-conversion in silicon solar cells and the design of reliable Si-MEMS structures.

LIST OF PUBLICATIONS

Textbook Chapters:

- **A. A. Fashina**, K. K. Adama, M. G. Zebaze, and W. O. Soboyejo "Improving the Performance of Light Trapping in Crystalline Silicon Solar Cell through Effective Surface Texturing" **Advanced Materials Research: Materials and Technologies for Sustainable Development**. Eds. W. Soboyejo, S. Odusanya, Z. Kana, N. Anuku, K. Malatesta And M. Dauda. Switzerland: Trans Tech Publications, Vol. 1132, pp 144-159: <http://dx.doi.org/10.4028/www.scientific.net/AMR.1132.144>

Peer-Reviewed Journal Articles:

- **A. A. Fashina**, M. G. Zebaze Kana and W. O. Soboyejo, "Optical Reflectance of Alkali-Textured Silicon Wafers with Pyramidal Facets: 2D Analytical Model" *JMR* **30(7)**, **904-913**, **2015**; doi: 10.1557/jmr.2015.70.
- **A. A. Fashina**, K. K. Adama, O. K. Oyewole, V. C. Anye, J. Asare, M. G. Zebaze Kana and W. O. Soboyejo, "Surface Texture and Optical Properties of Crystalline Silicon Substrates." *JRSE* **7(6)**, **063119**, **2015**; <http://dx.doi.org/10.1063/1.4937117>.
- **A. A. Fashina**, J. Asare, C. J. Ani, O. K. Oyewole, V. C. Anye, M. G. Zebaze Kana and W. O. Soboyejo, "Modelling of Fatigue Failure in Silicon MEMS Structures." (Under Review).
- T. M. Tong, J. Asare, E. R. Rwenyagila, V. Anye, O. K. Oyewole, **A. A. Fashina** and W. O. Soboyejo, "A Study of Factors that Influence the Adoption of Solar Powered Lanterns in a Rural Village in Kenya" *PGDT* **14(4)**, **448-491**, **2015**.
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LIST OF CONFERENCE PRESENTATIONS

14th International Union of Materials Research Societies – International Conference on Advanced Materials (IUMRS-ICAM): ICC Jeju, South Korea.

“On the Effect of Stress-Assisted Dissolution of Topical Silica Layer on the Fatigue Failure in Poly-silicon MEMS Structures”

Presentation, October 2015.

1st AUSTECH Conference: African University of Sci. and Tech. Abuja Nigeria.

“On the Reliability and Performance of Solar Powered Street Lighting Systems in Nigeria: Taking AUST-Abuja as a Case Study”

Presentation, October 2015.

1st AUST PhD. Colloquium: African University of Sci. and Tech. Abuja, Nigeria.

“On the Effect of Surface Texture and Nanoscale Surface Oxides on the Optical and Mechanical Properties of Silicon Single Crystals and MEMS Thin Films”

Presentation, January 2015.

7th African Materials Research Society Conference: Addis-Ababa, Ethiopia.

“Theoretical Analysis of the Optical and Light Trapping Behaviour of Alkali Textured Silicon Wafers”

Presentation, December 2013.

12th Nigerian Materials Congress (NIMACON): Abuja, Nigeria.

“Analytical Model of Light Interaction with Textured Pyramidal Structures”

Poster, November 2013.

11th Nigerian Materials Congress (NIMACON): Ile-Ife, Nigeria.

“Atomic Force Microscopy Analyses of Textured Silicon Wafers for Solar Cell Applications”

Presentation, November 2012.

ACKNOWLEDGEMENTS

It is expedient on my part to give praise, honour, glory and adoration to the Almighty God, who has sailed me through the turbulent wave of challenges and difficulties that might have been involved in the completion of this research work, so glory to the supreme most “OLODUNMARE, THE ALEWILESE OBA MIMO”.

Many people encouraged me in various ways to the realization of a successful completion of this research work, and I would be doing injustice to my conscience if I fail to express my profound gratitude to them.

My sincere appreciation goes to my Advisor, Professor Winston Oluwole Soboyejo for his influential support, encouragement and useful suggestions given to me in the course of carrying out this research work. Your invaluable inspiration and tireless pursuit of academic excellence at AUST and the world at large has provided me with the opportunities I never could have dreamed of. You are not just an adviser, but more of a mentor to me.

Special thanks to my co-advisor, Dr. M. G. Zebaze Kana. Your speedy problem-solving and comprehensive experience of measurement methods and solar cell technology was invaluable for all the experimental work presented in my fourth chapter.

I am grateful to thank Professor Terry Alford, Professor Oleg Yordanov and Dr. Omololu Akin-Ojo, for generously serving on my PhD. committee. Your reviews, comments, suggestions and valuable feedbacks are much appreciated.

Thanks to the Head of Department of the Physics stream, Dr. Omololu Akin-Ojo, for his continuous help and support in the department. His enthusiasm for new ideas was particularly inspirational.

I also acknowledge the entire academic and non-academic staff of AUST whose contributions in one way or the other made possible the successful completion of my graduate studies at AUST.

Regarding the experimental part of this work I owe many thanks to O. Oladipupo for being enthusiastic about practically all my experimental works at SHESTCO and I also acknowledge Seye for his assistance in preparing etchant concentration in CAL. The woman responsible for the good results with the spectrometer is Mrs Onugu K. Oluchukwu, I say a big thank you. Of course I gratefully acknowledge Engr. Adama K. for help with numerous experiments in the Physics Advance Lab (SHESTCO). Not forgetting Dr. Sola Odusanya for his support during my stay in SHESTCO Staff's quarters. I also recognize the efforts of other staff of SHESTCO PAL whose assistance in preparing samples and conducting test was crucial.

The completion of my fourth chapter would not have been possible without the cooperation of the Soboyejo research group while at Princeton University, particularly, Dr. Tiffany Tong, Dr. Ji Du, Dr. Nicolas Anukwu and Dr. Karen Maletesta. Thank you for your hospitality.

Furthermore, my profound gratitude goes to my parents Mr. & Mrs. S. A. Fashina for their parental care, financial and spiritual support during the course of my study. And to my brothers Ayodele, Babajide, Ayoola, Adedayo and Ayokunle I said a big thank for your moral and financial support.

My special thanks goes to the following peoples whom in one way or the other had made a great contribution to the successful completion of this work: Dr. & Mrs. Peterside, Mrs. Adejumo, Mrs. T. Oluwashina, Bolade Igbabo, Mr. Ebenezer Annan, Otura Annoh B., Azeko T. Salifu, Adoga Abel, Dahiru Sanni, Mrs. N. Joseph, Mustapha K., Mr. Caleb Ede, Mr. Daniel Akinola, Mr. Dauad Ibrahim, Ampaw Edward, Yusuf Shaidu, Mr. & Mrs. Oyelami, Onoja Joseph, Mr. Raji, Dcn. Mike, Dcn. Oladokun, Dcn. Richard, Dcn Emeka, A. Saheed, F. Mayowa, Danyuo Y., Joseph O. Uduma, Blessing Omaji, Mrs. O. Deborah Oyewole, Mrs Umwana Iwok, Ebere George, Mr Komolafe and Dr Joseph Berry (NREL).

I will like to acknowledge Bruno Dandogbessi and Uche Opara for useful scientific discussions and valuable input that are evident in my third chapter. My appreciation is also extended to the World Bank STEP-B Program, the World Bank African Centers of Excellence Program, the African Development Bank, the African Capacity Building Foundation (ACBF) and the Nelson Mandela Institute for their financial support.

I would also particularly like to thank Damilola Momodu (senior man); having you around made my access to scientific journals easy. For additional help during the crucial writing phase, I would like to thank David Clement and Omotoba Oladele for their great influence to this work. For a nice working atmosphere I would like to thank the Soboyejo research group at AUST particularly the solar energy research group.

Finally, my thanks go to my colleagues, Ani Emeka and Joseph Asare for their extensive insights into FEM simulation and into ABAQUS software detail.

I apologize for anyone's name that might be missing at one point or the other. Nevertheless, words cannot justify my profound gratitude for all of you.

I say thanks to you all. God bless (Amen).

Fashina Adebayo Adeboye

AUST, Abuja,

Nigeria, 2015

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CHAPTER ONE

INTRODUCTION

1.1 Background

Silicon (Si) is one of the most abundant of elements and an essential ingredient of a large number of minerals that make up the Earth's surface [1]. It was first isolated in 1824 by the Swedish chemist Jöns Jacob Berzelius who also discovered Cerium, Selenium and Thorium [2, 3]. Crystalline silicon was first produced in 1854 by Henri Deville using electrolysis [3]. Since that time, it has been the most important element used in the semiconductor industry [4]. Without a supply of this important element, it would be impossible to make the range of high quality computers, calculators, cell phones, radios, *etc.* It is, therefore, a key element that modern industrial societies rely upon.

Silicon is used in various ways in microelectronics such as computer chips, with one example being the metal-oxide-semiconductor field effect transistor (MOSFET), the basic switch in modern electronics and computing [4, 5]. It is also used in photoelectric cells in solar panels to convert solar energy to electrical energy for use in both terrestrial and space applications such as space-crafts, satellites, electronic watches and pocket-sized solar calculators, transistors, lighting and the provision of other sources of energy [4, 5].

Today's silicon research spans the full range from idealized models to realistic models across different industries [5]. The solar and micro-electro-mechanical systems (MEMS) industries are few among many other that have benefited from intensive research on silicon and its applications [5-7]. In any case, silicon research has improved the performance of several microelectronic products [4-8].

1.1.1 Importance and Prospects of Silicon-based Solar Cells.

Silicon can be used to make Photovoltaics (PVs). Photovoltaics are devices that convert solar energy directly into electrical energy [9]. They are promising, renewable, almost unlimited, and environmentally friendly [9]. The development of photovoltaics is imperative today because of the gradual depletion of the earth's fossil fuels. The increased use of photovoltaics could also result in a reduction in the emission of heat trapping "greenhouse gases" [10] that are emitted by traditional power plants.

Currently, silicon-based solar cells are the most widely used commercial photovoltaics in the world [11]. The PV market, dominated by crystalline silicon, has grown by more than 20% per year on average over the past 15 years. However, PVs faces the problem of profitability, as they must compete with traditional sources and methods of energy conversion [12]. To become competitive, PV modules must achieve stable conversion efficiencies more than fifteen percent; have lifetime of at least thirty years, and cost about \$US 0.4 per peak Watt or less [13].

The low efficiency-to-cost ratio of solar cells is one of the main problems that prevent the widespread use of PVs in wide-scale terrestrial applications. For such applications, lower cost materials are needed that are much less expensive than single crystal silicon. Large scale manufacturing of such materials is also needed. However, the ultimate success of silicon photovoltaic cell technology requires significant cost reduction and improvements in photo-conversion efficiency. One approach that can simultaneously achieve these two objectives is the use of light-trapping.

1.1.2 Surface Texturing and Light Trapping

In recent years, silicon-based solar cells have dominated the solar cell industry across the world [11]. They currently account for about 90% of all the solar panels that are sold globally [14]. In such panels, the absorption of sunlight is relatively weak [15]. This is due to

the optical losses that occur due to the high refractive index (approximately 3.5) of crystalline silicon at solar wavelengths [15]. Furthermore, about 35% of the incident light is reflected back from the silicon surface (see Figure 1.1a). This reduces the efficiencies of single junction crystalline silicon solar cells to levels between ~12 and 20% [16]. Hence, in order to increase the efficiency of the silicon-based cells, there is a need to reduce the optical reflectance of silicon wafers, especially for wavelengths in the visible spectrum. This need has stimulated the silicon solar research community to explore numerous reflection-reducing techniques over the past 45 years [14-18].

In most cases, the reflection reduction techniques have been termed light trapping. Light trapping allows photons to spend more time in the solar cells (see Figure 1.1b), compared to the absorption time [19]. Light trapping in silicon solar cells can be achieved in two main ways. The first being the reduction of front surface reflection (i.e. surface texturing); while, the second involves increasing the optical path length of light within the cell [20]. In any case, surface texturing represents a promising approach for the engineering of surface reflection and light absorption by silicon solar cells.

Surface texturing involves the control of surface geometry for the reduction of surface reflection on crystalline silicon substrates [21]. It is often achieved by the anisotropic etching of (100)-oriented silicon substrates with potassium hydroxide (KOH) and isopropyl alcohol (IPA) solutions [18]. This generally results in the formation of square-based pyramidal micro structures [22]. The sizes and uniformities of the resulting pyramids are traceable to isopropyl alcohol (IPA), which acts as a wetting agent, when added to alkaline etchants [23].

However, the role of IPA in alkaline texturing process is not fully understood, in spite of several attempts to explain its effect on silicon wafers [24, 25]. Nevertheless, prior works have explored the effects of KOH and IPA etching on the morphology of silicon wafers [26,

27]. Furthermore, these studies have not established the ratios of IPA to KOH that are needed for the control of silicon surface textures that minimize the reflection of incident sunlight, while trapping the light for photoelectric conversion.

1.1.3 Importance and Prospects of Silicon Micro-Electro-Mechanical-Systems

Apart from photovoltaics, another area in which silicon has found application is in micro-electro-mechanical-systems (MEMS). There has been increased interest in the application of MEMS in recent years [6-8]. These applications include: biological sensors in the human body, hydrostats, pressure sensors, inertial sensors, ink jet cartridge nozzles, pressure transducers, linear racks, accelerometers and actuators [6-8]. However, the reliability of these devices is a strong function of the type of loading and the environment [28].

Consequently, the performance and reliability of MEMS structures are frequently affected by cyclic loading and the environment. The engineering design of reliability, therefore, requires models that account for the time- and cycle-dependent degradation of MEMS materials. However, most MEMS materials undergo failure when subjected to cyclic stresses. This occurs due to a phenomenon known as “*fatigue*”. Fatigue is the most commonly experienced form of structural failure [28], yet surprisingly it is one of the least understood [28].

The pioneering work on the cyclic fatigue of Si MEMS structures was done by Connally and Brown [29]. Using cantilevered bend structures, they obtained stress-life and fatigue crack growth rate data that suggested a strong influence of water vapor on the fatigue of silicon. More recently, different research groups have examined and reported on the experimental and analytical/computational studies of the fatigue behavior of both single crystal [30] and polycrystalline silicon [31].

Like Connally and Brown, other researchers used silicon specimens fabricated by silicon micromachining technology which allows external [32] and integrated [33, 34]

loading. Prior work on the fatigue of silicon has resulted in a number of models of fatigue in silicon MEMS structures [31, 33-37]. The studies suggest: an increase in high-cycle fatigue lifetime with decreasing peak stress [35]; the dependence of fatigue on the cyclic stress levels, but not cyclic frequency [32]; morphological changes in the surface silica during fatigue [36]; and the possible growth of surface cracks due to slow crack growth [38].

Despite the extensive research on the design and characterization of various properties of MEMS structures, there is still no consensus on the mechanism of fatigue in silicon MEMS structures [39]. Some researchers suggest that silicon MEMS fatigue occurs due to the growth of surface perturbations until they evolve into cracks (Figure 1.2) [37, 38]. In this case, the topical oxides also appear to thicken during cyclic loading, (Figure 1.2) [39-41]. Others suggest that cracks formed during fabrication can extend by slow crack growth when the crack driving force exceeds a critical value [38]. There is, therefore, a need for further work to establish the mechanisms of fatigue in silicon MEMS structures.

1.2 Motivation

The motivation for this thesis comes from the need:

1. To increase the light absorption within silicon solar cells for the enhancement of photoelectric conversion;
2. For improved understanding of the role of stress-assisted dissolution on the possible formation and growth of cracks in Si-MEMS structures;
3. To model the potential role of slow crack growth in the fatigue of silicon MEMS structures.

1.3 Objectives

The primary objective of this research is to provide improved understanding of the effects of surface texture on the optical properties of silicon structures that are used for silicon solar

cells. The underlying mechanisms of fatigue are also elucidated for Si MEMS structures. The research aims are to:

1. Explore the effects of KOH/IPA etching on the stability of pyramidal textures on the (001)-oriented silicon wafers;
2. Explore the effects of etchant concentration and KOH/IPA ratio on the optical properties of textured silicon surfaces, along with the effects of etching duration and temperature;
3. Study the reflection behavior of textured silicon surfaces under non-normal incidence.
4. Investigate the possibility of secondary reflection, for the full range of incidence angles to the substrate using an analytical approach;
5. Validate predictions from analytical model with experimental measurements of reflectance from (001)-textured silicon surfaces;
6. Elucidate the role of stress-assisted dissolution on the possible formation and growth of cracks;
7. Compare results from the stress-assisted dissolution model with measured surface profiles from prior work.

1.4 Organization of the Dissertation

In chapter 1, the background/introduction to the work on silicon surface texture and silicon MEMS fatigue is presented.

In chapter 2, the relevant literature on silicon surface texturing and silicon MEMS fatigue are presented. The basic concepts of surface texturing and the optical properties of silicon wafers are discussed. This is followed by the description of the methods of implementing light trapping in silicon solar cells before assessing the light trapping effects in

prior works. The MEMS testing techniques and fatigue mechanisms (in Si MEMS structures) are also elucidated.

Subsequently, chapter 3 presents an analytical model of the reflectance of flat and textured silicon substrates. The reflection behavior of textured silicon surfaces is modeled under non-normal incidence. The model was used to determine how incident light interacts with textured micro-pyramidal facets on alkali-textured silicon surfaces. The dependence of the secondary reflection on the angles of incidence of light rays is explored, along with the contributions of the primary and secondary reflection to the total reflection. The possible optical interactions are considered for a range of pyramidal geometries and light incidence angles. The analytical model is then used to determine the reflectance values of well controlled textured surfaces and validated with experiments. The potential for light trapping is also explored, before discussing the implications of the results for the design of micro-textured silicon surfaces.

In chapter 4, the results of an experimental study of the effects of surface texture on the optical and light trapping properties of silicon wafers are presented. A combination of profilometry, optical microscopy, scanning electron microscopy (SEM) and atomic force microscopy (AFM) is used to study the effects of KOH/IPA etching on the morphology and roughness of the textured surfaces. The resulting reductions in surface reflectance associated with controlled etching of (100)-oriented silicon wafers with KOH: IPA mixtures are explored alongside with the light trapping effect of textured silicon surfaces produced. The implications of the results are then discussed for the design of light trapping in silicon solar cells.

Chapter 5 presents the combined results of analytical and computational study of the mechanism of fatigue in Si-MEMS structures. To examine the effect of the stress-assisted dissolution on the possible formation and growth of cracks, finite element analysis was performed for topical SiO₂ layer on the silicon structures using ABAQUS FEM software. The

possible formation and growth of cracks by such dissolution was elucidated and compared with measured surface profiles from prior work. The measured surface topologies obtained using atomic force microscopy (AFM) are also compared with predictions from linear perturbation analysis of the stability of surface topology that evolves during stress-assisted dissolution of the silica layer.

Finally, chapter 6 presents conclusions from this current study, along with suggestions for future research.

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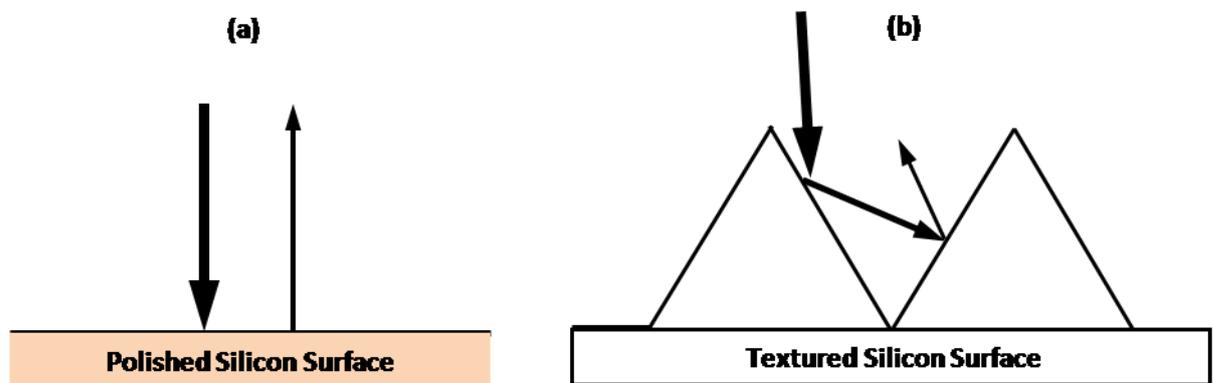


Figure 1.1: Schematic of light interactions with silicon surfaces: (a) about 35% of the incident light is lost on polished silicon surface; (b) incident light has a second chance to be absorbed on textured silicon surface

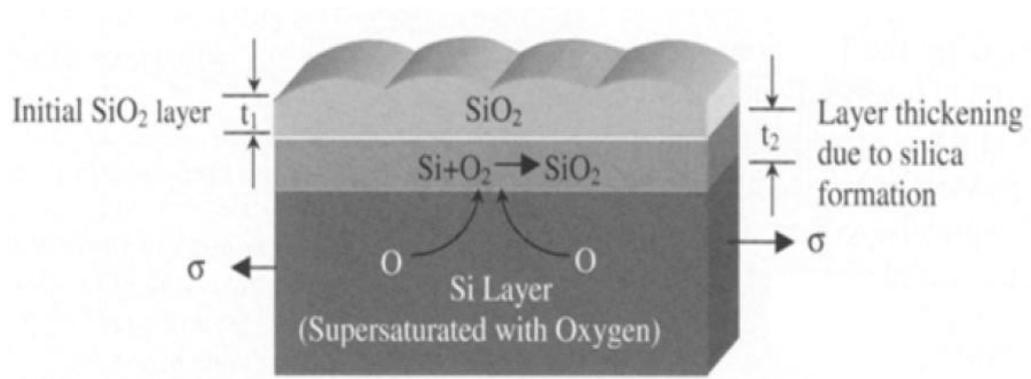


Figure 1.2: Oxide Thickening Mechanism. Taken from Ref. [41]

CHAPTER TWO

BACKGROUND THEORY AND LITERATURE REVIEW

2.1 Introduction

Silicon-based solar cells are one important class of photovoltaics that are currently the subject of intense research, development, and commercialization efforts [1]. This is due to its semi-conductive properties [1, 2]. However, silicon can be made conductive by doping it with boron, gallium, phosphorus or arsenic [1]. This has been a useful technology that is mostly used in computer chips and micro-electro-mechanical systems [2]. Furthermore, it is well established that the optical properties of flat crystalline silicon surface is limited by its high refractive index (approximately 3.5) [3]. About 35% of the incident light is reflected back from the silicon surface [4]. This reduces the efficiencies of crystalline silicon solar cells to the levels between ~12 and 20% [4]. This is why the photovoltaic research community has been exploring numerous reflection-reducing techniques in the last 45 years [4-8]. One of the ways to achieving reflection-reduction in silicon is surface texturing. Hence, a review of surface texturing is presented in the subsequent sections.

In semiconductor/micro-electro-mechanical-systems (MEMS) manufacturing, silicon is a material of choice due to its strength (1-4.3 GPa) and its mature fabrication technique [9-11]. This has led to the growth of MEMS applications that includes micro-sensors and micro-actuators [10]. In spite of this, silicon has relatively low fracture toughness (~1 MPa \sqrt{m}) [12-16] that allows it undergo crack-induced failure under ambient conditions [10, 12, 17-20] when in bulk form. However, the underlying mechanisms of sub-critical cracking are not fully understood [15]. Some researcher suggest that this is due to slow crack growth process [18, 19], while others suggest a significant role of stress-assisted dissolution by water

or water vapor in the atmosphere [10]. These potential mechanisms will be discussed in section 2.7 of this chapter.

This chapter is divided into seven sections. Following the introductory section, section 2 presents the basic concept of surface texturing and optical properties of silicon. This is followed by Section 3, in which the chemical etching in silicon solar cells are described. The early studies of light trapping in silicon solar cells are presented and discussed in Section 4 while in section 5, the methods of implementing light trapping in silicon solar cells are described before assessing the light trapping effects in prior works. Furthermore, section 6 presents the theory of determining the heights and tilt angle of pyramids produced by KOH texturing of silicon wafers. Finally, the testing techniques and mechanisms of fatigue in single-crystal and polycrystalline silicon are discussed in Section 7.

2.2 Basic Concept of Surface Texturing and Optical Properties of Silicon

2.2.1 Surface Texturing of Silicon

Surface texturing has long been used as a reflection-reducing technique in silicon solar cells since the mid-1970s [8]. Surface texturing may be thought of in a more general way as the roughening of silicon surface to redirect light. It involves the control of surface morphology by etching [21], photolithography [22] or laser-based [23] techniques that can be used to control the interactions of light with silicon surfaces. However, the wet chemical etching in an alkaline solution is the most common method used in the solar industry [24]. This process is referred to as anisotropic etching. Furthermore, the resulting morphology depends on the etch rate between the different crystal planes and the wafer orientation.

Consequently, for effective light absorption in silicon solar cells, (100)-oriented substrates are preferable [2]. This is due to the fact that the interactions between the alkaline solution and silicon surfaces form square-based pyramids. Although, the pyramidal structures

can vary, the distribution and uniformity can be reduced by controlling the texturing process parameters: etch time, etch temperature, etchants *etc.* [25]. This allows the light interactions with the pyramidal facets at different incident angles to be redirected to produce multiple reflections that can increase the possibility of light absorption within silicon substrates. The schematic illustration of the light interaction and the SEM image of such pyramidal structures are presented in Figure 2.1. This type of surface texturing is mostly referred to as "*random pyramid*".

2.2.2 Optical Properties of silicon

2.2.2.1 Refractive Index

Light travels at 3.0×10^8 m/s in free space [26], but in other media it travels more slowly. This is a consequence of the photon interactions at the atomic level and results in the difference in refraction index of the media when compared to that of free space. At the macroscopic level, the interaction of light with matter comprises of four components: an incident, a reflected, a transmitted, and an absorbed (or scattered) component [26]. Depending on the properties of the material, when light travels between two optical media of different refractive indices, there are possibilities that the interface experience all four component of interaction or less.

Furthermore, high reflection at the interface of two optical media can be traced to a mismatch in refractive index. This has been explained by Augustin-Jean Fresnel [27] using the Fresnel equations to describe the behavior of light rays that travel between media of different refractive indices [27]. Moreover, all commonly used cell absorbing materials such as cadmium telluride copper indium and silicon demonstrates relatively high refractive index. For example, the refractive index of bare silicon is about 3.5. This causes about 35% of the incident light that strikes its surface to be reflected with the reminder transmitted through the interface before it possibly absorbed [4]. In determining the optical properties of silicon, its

refractive index places a key role and can thus be defined as the ratio of the speed of light, c , in free space to its speed, v , in the silicon material. This is given by the expression [26]:

$$N = \frac{c}{v} \quad (2.1)$$

Nevertheless, the refractive index is usually a complex number with a real and imaginary part and can be expressed as [26]:

$$N = n - i * k \quad (2.2)$$

where n is the real refractive index, k , is the extinction coefficient (damping constant) and i is the imaginary unit. Figure 2.2 presents the dependence of n and k on the wavelength in silicon. However, the following section describes how the refractive index of silicon contributes to its reflection and absorption.

2.2.2.2 Reflection and Absorption

(A) Reflection

When light strikes the interface of two media, a fraction of the incident light is reflected back into the first medium and the remainder is absorbed or transmitted into the second medium [26]. This applies to cell absorbing materials, including silicon [2]. As stated in the preceding section, the fraction of light that is reflected, transmitted or absorbed depends on the thickness of the media, refractive index of the media and in addition the angle of incidence on the interface of the media among others factors [26, 27]. Nevertheless, the index of refraction is dependent on wavelength and so zero reflection can only occur at a single wavelength. Within this context, the photovoltaic industry, carefully choose the refractive index and thickness of silicon to minimize reflection for a wavelength close to the peak power of solar spectrum (0.6 μm) [28]. However, the reflectance (R) can be defined in terms of the index of refraction of the media on either side of the interface as expressed in Equation 2.3 [26]:

$$\mathcal{R} = \frac{(n_{Si} - n_{Air})^2}{(n_{Si} + n_{Air})^2} \quad (2.3)$$

where the index of refraction of the silicon is n_{Si} and the index of refraction of air is n_{Air} .

If the refractive index of air is approximately equal to 1, then Equation 2.3 becomes:

$$\mathcal{R} = \frac{(n-1)^2}{(n+1)^2} \quad (2.4)$$

Furthermore, Equation 2.4 can then be used to calculate the reflectivity of light on bare silicon in air. This is presented in Figure 2.3 for normally incidence of light at different wavelengths.

(B) Absorption

In semiconductors, absorption occurs when an electron absorbs a photon [28]. Although, photons also have the option of being transmitted through the silicon cells or reflected away from the silicon surface, transmitted or reflected light is considered a loss in silicon technology [2, 28]. This makes optical science extremely important when minimizing the percentage of reflected light needed to optimize the absorption within the silicon substrates. For example, 35% of light is reflected away from silicon surfaces at wavelengths relevant to solar applications (Figure 2.3), a number which greatly hinders absorption and subsequently the overall efficiency of the system [28, 29]. However, the absorption rate of photons is proportional to the intensity for a given wavelength. This implies that, as light ray is transmitted through a material, the flux of photons (intensity) reduces exponentially as part of the photons are been absorbed [28]. Therefore, the amount of photons that attains a particular point in the semiconductor depends on both the wavelength of the photon and the thickness of the semiconductor materials. The exponential decay of **monochromatic** light can be modeled for semiconductor materials (silicon in this case) using the Beer-Lambert law [28] as expressed in Equation 2.5:

$$F(x) = F(x_0)e^{-\alpha(x-x_0)} \quad (2.5)$$

where $F(x)$ is the intensity at a point x below the silicon surface, $F(x_0)$ is the intensity at a point x_0 on the silicon surface, and α is the **absorption coefficient**.

An absorption coefficient, α , determines the depth at which light of a particular wavelength enters into the silicon surface. It is related to another quantity known as the **extinction coefficient** (κ), an optical property of the semiconductor material that is related to the index of refraction n . It simply determines how much light is absorbed by the material. For example, when $\kappa > 0$, it implies that there is light absorption and when $\kappa = 0$, it implies that light travels straight through the material (no absorption). The absorption and extinction coefficients are both related to the wavelength of light and their relationship can be expressed as [28]:

$$\alpha = \frac{4\pi f \kappa}{c} \quad (2.6)$$

where f is the frequency of the monochromatic light (related to the wavelength by $\lambda=v/f$, where v is the velocity of the light wave), c is the speed of light, and π is a constant (≈ 3.14).

Figure 2.4 presents the absorption coefficient of silicon as a function of wavelength. Materials with high extinction coefficients are able to absorb light much more easily than materials with low extinction coefficients.

2.3 Chemical Etching in Silicon Solar Cells

2.3.1 Overview

Wet chemical etching is regular technique used in the solar cell industry for surface texturing of silicon surfaces [30, 31]. It is classified into isotropic and anisotropy etching. In Isotropic etching, etch rate are the same in all directions and does not depend upon the

orientation of the mask edge while anisotropy etching depends upon orientation of crystalline planes and the orientation of mask edge. The details of the mask pattern also determine the final etched shape. This implies that the geometry of the resulting texture depends strongly upon the nature of anisotropic etching process.

Potassium hydroxide (KOH) and Sodium hydroxide (NaOH) are the two most common alkaline etchants used for the anisotropic etching of silicon surfaces. They are used largely because of their relatively low cost, and the high capacity of anisotropically etched surfaces for light trapping [30, 32-37]. However, the effects of anisotropic etching on the morphology of silicon surfaces also depend strongly on wafer orientation as was introduced in the preceding section [38]. Consequently, substrates with (100), (110) and (111) orientations are largely relied upon by silicon solar industry [7]. Nevertheless, (100) wafers are the most geometrically appealing, since the orientations of {111} planes can be easily located on them [7]. This section presents an overview of anisotropic etching method and its resulting optical and morphological effects.

2.3.2 Alkaline Etching

KOH anisotropic etching of silicon is an alkaline-based etching technique that is mainly referred to as the direction-dependent etching of silicon. One notable advantage of alkaline etching over other etching method is that it can be used to control or reproduce different kind of geometry on silicon surfaces. This is as a result of the strong dependence of its etching rate on crystal direction and on etchant concentration. Hence, anisotropic etching of (100) silicon has been a key process in silicon-based solar cells.

In the late sixties, Finne [39] and Price [40] made the first attempts to etch silicon. In 1967, Price [40] used the potassium hydroxide (KOH), water (H₂O) and isopropyl alcohol (IPA) as the first etch solution to etch silicon. By 1969, Lee [41] introduced a ternary liquid

containing hydrazine, isopropyl alcohol and water as etch solution for silicon. He chose Hydrazine as an oxidant, IPA as a complexing agent, and water as a catalyst. The effect of the etch solution was used to show the anisotropic and selective characteristics of alkaline etching. He explained the dependence of the etch rate on the crystal orientation as anisotropic and described the dependence of the etch rate on the doping concentration of silicon as the selective characteristic. Consequently, this fundamental knowledge has been used to produce variety of microstructures in the microelectronic and micromechanical industries [42].

Moreover, in the same year, Haynos *et al.* [43] first introduced Lee's etching technique to the photovoltaic industry for mono-silicon substrates [43]. Nevertheless, the etch solution introduced by Price [40] has been employed by the photovoltaic industry since it was first introduced in 1967. It has long become a standard (KOH-IPA standard) used to texture silicon surfaces. It worked very well for a long time before the development of the sawing methods where different chemicals are now used to clean native oxides from the sawed wafers. This process changes the surface characteristics of the as-cut silicon wafers and thus reduces the effectiveness of the KOH-IPA solution [44]. Subsequently, there has been some disagreement as to what the active etching species is. In a study by Palik *et al.* [45] in 1983, OH⁻ ions were found to play the key role in the etching process of silicon surfaces. They observed that IPA does not appear to take part in the etching process and thus contradicting the observations of Lee [41] and other authors who believe IPA has great influence on the etching process [46].

Furthermore, Seidel [47] also assumed the effect of IPA to be minimal despite the considerable decrease in the etch rate of silicon when its concentration is increased. In more comprehensive study by Seidel in 1990 [48], he explained that IPA act as a mask against chemical reactants and it is preferentially absorbed on (111) planes to form pyramidal structures. He further explained that IPA regulates the etching rate for KOH-IPA solutions at

constant KOH concentration and temperature. This allows it to attract water molecules around itself and thus controlling the water concentration in the solution. In 1993, Elwenspoek [49] proposed a new theory to explain the mechanism of anisotropic silicon etching that was inspired by the theories of crystal growth. He suggested that the anisotropic nature of etch rates and activation energies ultimately depends on the physical state of the silicon surfaces. Kenji *et al.* [50] also predicted that the etched silicon surface can be smoothen by increasing both the KOH concentration and etch temperature [50].

Several researchers also investigated on the effect of the texturing process parameters on the formation of pyramidal textures on (100) textured silicon surface using various alkaline etching techniques [51-54]. In a recent work, Xun *et al.* [51] suggested that the sizes and uniformities of pyramidal structures are traceable to the isopropyl alcohol (IPA) which confirms the work by Siedel [48]. However, the role of IPA in alkaline texturing process is not fully understood, in spite of several attempts to explain its effect on silicon wafers [32, 51]. Nevertheless, prior work has explored the effects of KOH and IPA etching on the morphology of silicon wafers [33, 51-53]. However, these studies have not established the ratios of IPA to KOH that are needed for the control of silicon surface textures that minimize the reflection of incident sunlight, while trapping the light for photoelectric conversion. Therefore, more experimental results under various process conditions are required to improve on the existing physical models. The experimental results of this current research are discussed in chapter four.

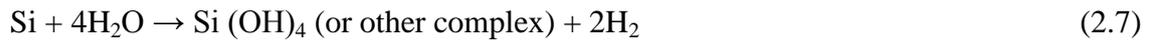
2.3.3 Etch Reaction/Etch Anisotropy

The anisotropy nature of silicon depends greatly on its crystallographic properties. This allows the growth of silicon and its etching anisotropic in nature. This is the reason KOH anisotropic wet etching is able to produce the 3-D micro-structure. Nevertheless, the etch anisotropy of silicon can be simply examined by comparing the etch rates of various

crystal orientations of silicon at specific etchant composition. Reports for prior work, has shown that the etch ratios varies considerably. J. B. Price [40] reports the etch ratio for {100} to {111} planes that was etch in KOH solution of 10-15 weight percent to be 35:1. A higher etch ratio of 300:600:1 for {110} to {100} to {111} planes have also been reported for more concentrated solutions [55]. Also, an etch-rate ratio 160:100:1 is found for {110} to {100} to {111} planes at 20°C and decreases to 50:30:1 at a higher temperature of 100°C. Conversely, a higher etch ratio of 400:200:1 at a temperature of 85°C has been recorded by Kendall [56].

Furthermore, it has been shown from prior works that the silicon surface is hydrogen terminated during the alkaline etching [57-61]. Although, there have been some disagreement to what the active etching is, some investigation refer to OH⁻ as the active etching species [30, 45] while others refer to water [57, 58]. This is illustrated in Equations 2.7-2.10. However, it has been established from prior works that the reaction products of the etching of silicon include a silicon hydroxide complex (Si(OH)₄), and a released hydrogen gas [39,45,62].

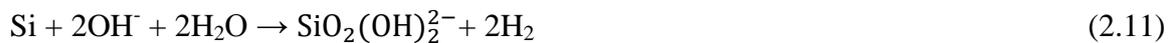
In general, the overall reaction where water is accepted as the active species [57, 58] is given by:



Also, the (electrochemical) reaction with OH⁻ as the active species [17, 18] is given by:



In a more detailed form, Seidel *et al* state the gross reaction as [63]:



2.3.4 Pyramidal Textures

Pyramidal texture formed on silicon surfaces by alkaline etching has been proven to be an important and effective way for reflection reduction in silicon-based solar cells [64]. During wet anisotropic etching of (001) substrates, grooves with {111} sidewalls are exposed to form square-based pyramids [25]. Such pyramidal structures are formed as a result of interactions between the alkaline solutions and silicon surfaces along {111} planes [37]. The pyramids that are produced are with apex angles of 70.6° and facet tilt angles of 54.7° for an ideal process [53, 65]. However, for actual industrial c-Si solar cells, where non-ideal etching is observed, a slightly smaller base angle (or facet tilt angle) is normally observed [66, 67]. This has been shown to be less than 52° in Refs [66, 67].

Moreover, the sizes of the pyramids and its uniformity are mostly randomly distributed and can affect the optical performance of the solar cells [64, 68]. Consequently, the reflectance value for textured silicon surfaces becomes about 20% lower than that of the polished silicon surfaces. Usually, the average pyramidal size varies between $1\ \mu\text{m}$ and $9\ \mu\text{m}$ with a corresponding reflectance value ranging from 14-15% [20, 70-72]. However, the stability (uniform distribution) of pyramidal textures on silicon surfaces is not well understood. In prior work, IPA is frequently added to the alkaline solution to keep the concentration constant and thus maintaining stability during the etching process [32]. This is due to the temperature at which IPA evaporates [32].

Furthermore, in recent years, researchers have shifted focus to investigating new texturing methods and finding alternative solutions. Nishimoto and Vallejo used sodium carbonate solution (without adding IPA) to etch silicon wafers [73, 74]. The resulting pyramidal structure from their work falls between the range of $4\ \mu\text{m}$ and $7\ \mu\text{m}$. In another work, Chu obtained a pyramidal structure with pyramid size of $6\ \mu\text{m}$ to $9\ \mu\text{m}$ by using a metal grid with suitable openings on silicon surface to confine the hydrogen bubbles [75, 76].

Nevertheless, he found it very difficult to produce metal grids of large-area and to control the distance between the grid and silicon wafers. Chen also used reactive ion etching (RIE) method to achieve low reflectance values from a uniform pyramidal structures with a pyramid size of $1\ \mu\text{m}$ [77]. Mavrokefalos synthesized inverted nanopyramid applicable for thin silicon films using standard scalable microfabrication techniques based on interference lithography and wet silicon etching [78]. Ordered pyramidal structures can also be fabricated by colloidal lithography with packed polystyrene spheres [79] or silica colloidal crystals as masks [80]. However, the process was complicated and needed expensive instruments.

2.3.5 Reflection Reduction by Alkaline Texture surfaces

The idea of reflection reduction by textured silicon surfaces was first suggested by Rudenberg *et al* [81] in 1961. They used mechanical texturing method to produce very low reflectance value without the use of anti-reflection coating. They observed that the pyramidal structures on the silicon wafers made the wafer dark grey/black in color and this they believed to have aid the reflection reduction. The work done by Rudenberg *et al* [81] however inspired the use of alkaline etchants for pyramid formation in the microelectronics industry, where microscopically smooth etch/growth textures are required on silicon. The initial experiments that were carried out for deliberate formation of pyramidal textures for solar cells employed alkali hydroxides such as KOH and NaOH [82]. This apparently leads to the exposure of intersecting slow etching $\{111\}$ facets yielding the pyramidal textures described previously. Following the assumption that the carbon contents in would induce the etching process and thus guarantee etching uniformity, an alcohol such as ethyl glycol [83] or IPA [84] is frequently employed. The square-based pyramids formed in these cases are usually seen to consist of ideal $\{111\}$ facets. However, more careful inspection of these pyramidal features generally suggests that some defects called the “hillock” are formed at the bottom of the pyramidal facets [85, 86-90]. Depending on the texturing process conditions, the hillocks

range from near-perfect upright pyramids with some slight bowing of the facets or beveling of edges [88] to features with distinctly octagonal bases [86]. Despite the accepted standard for the use of alkaline etching, particularly for pyramidal formation on (100) oriented monocrystalline silicon cells, the process parameters used and the resulting surface morphologies do not necessarily represent the only suitable conditions for achieving sufficient reflection reduction.

2.4 Early Studies on Light Trapping

2.4.1 Light Trapping in Silicon Solar Cells

Light trapping in semiconductor diodes was first suggested between 1968 and 1969 as an infrared absorption enhancement technique for silicon photodetectors [91, 92]. Although, there were other approaches to absorption enhancement within solar cells, most of the prior work were preceded by an early research on randomly roughened surfaces in 1974 by Redfield [93]. In his report, a simple and well defined geometrical scheme was designed to explain absorption enhancement in silicon cells. In the early 1980s, Goetzberger [94] and Yablonovitch [95] concurrently used Lambertian surface textures to describe various schemes built on randomizing the directions of incident light in solar cells [94, 95]. The application of both the Lambertian schemes and the well-defined geometrical features were visible in amorphous silicon alloy [96] and later in crystalline silicon solar cells [8].

Later in 1982, Yablonovitch and Cody [97] in a comprehensive work explored the light interactions with textured slab. They argued that internal scattering of incident lights occurs at random angles as a result of the textured slab [97]. They further explained that, when a perfectly reflective (white) sheet is used on the back surface, the internal light intensity is larger than the incident intensity by a factor of $2n^2$, where n is the wavelength dependent refractive index of the slab [97]. For an absorbing material, such as amorphous or crystalline

silicon, the enhancement of internal light intensity was found to be $4n^2$ [97]. This is a well established theoretical limit normally used for absorption enhancement in light trapping. However, a further study by J. Nelson [98] in 2003 showed that absorption can be enhanced by a factor of 10 in practice [98].

2.5 Methods of Implementing Light Trapping

2.5.1 Random Texturing

Random texturing is a promising light trapping technique has been shown it is experimentally appealing due to its cost effectiveness and ability to be achieved easily [2]. Also, modelling from prior work suggests the random texturing can effectively trap light [94]. This light trapping method is achieved either by Lambertian reflector, back reflector or a combination of front and back reflector. Goetzberger [94] established that the fraction of light reflected internally on Lambertian surface textures (diffuse reflector) made by random surface textures is equal to $1 - 1/n^2$, where n is the index of refractive index of silicon. Furthermore, about 90% of the weakly absorbed light from diffuse back reflector reflects internally from the surface of silicon material [8]. Yablonovitch and Cody [97] predicted that the optical path length can increase up to a 50-fold, when a front and back surface texturing is used for effective Lambertian reflection. Unfortunately, Lambertian reflector [8] has proved to be problematic experimentally. Nevertheless, random textures can be experimentally achieved for various level of effectiveness by reactive ion etching [99], photolithography [100], porous etching [101], or random-textured ancillary dielectric layers such as ZnO or SnO₂ [36].

2.5.2 Regular Structuring for Light Trapping

The regular structuring approach has been demonstrated in prior work for common light-trapping structures used in solar industry today (see Figure 2.5) [102]. Unlike random

texturing where the pyramids on the surfaces are non-patterned, regular structuring silicon surfaces are patterned into different shape [6]. These structures include upright pyramidal structures, inverted pyramidal structures, slats and perpendicular slats *etc.* The patterns are often achieved using the combination of photolithography and anisotropic etching [103, 104]. Moreover, the anisotropic nature of the alkaline solutions make the surface structuring possible for single-crystal silicon wafers [6].

The modelling and simulation of these geometrical structures is mostly carried out analytically using geometric optic or computationally using ray tracing techniques [105, 106]. Several simulations comparison on different metrics has been carried in prior work to evaluate the performance of these geometrics. This metrics includes path length enhancement, number of rays remaining trapped after each pass within the substrate, reflection from front surface, short-circuit current *etc.*

In general, comparison is mostly achieved by tracing a ray within the substrate and programs are based on Monte-Carlo simulation. This program includes RaySim6.0 [107], Texture [105], SunRays [108] *etc.* For accurate result in complex ray tracing analysis, no assumptions are made about the distribution of light within the absorber layer. As an alternative for less complex cases, the optical path for the characteristic incident rays of light are plotted using geometric optics to trace the pathway of light rays it is reflected and refracted at surfaces and interfaces. This approach is analytically useful for the analysis of regularly structured surfaces [109].

Consequently, the use of a textured front surface and an optical back reflector are the most common light trapping feature in silicon cells [94,97,110]. For an ideal case, Yablonoich [97, 95] has shown that a randomly textured front surface can be combined with a perfect back reflector to achieve a light trapping feature that can effectively enhance the

light intensity inside the silicon cell. However, in solar cells with a simple geometry, light rays enter the cell through the front surface and, if not absorbed, leave through the rear surface of the cell. Nevertheless, various schemes have been developed to improve the practical operation of silicon cells devices such as crystalline [104], polycrystalline [100, 111] and amorphous [110] silicon cells.

Furthermore, light trapping can be used to reduce the cell thickness without reducing the absorption of light within the crystalline or amorphous silicon solar cells [103] Light trapping can also be used to enhance the open circuit voltage [112, 113].

2.5.3 Assessment of Light-Trapping Effects in Previous Work Done

2.5.3.1 Lambertian Surface Limit and Yablonovitch Limit

Lambertian surface also known as diffusion surface is one that allow light rays to be reflected in randomly in all directions. The light rays are scattered adjacently to the surface at all possible range of angles (see Figure 2.6). The purpose of this is to however enhance the light absorption within a randomly textured material. Campbell *et al* [8] demonstrated that the path length enhancement of weakly absorbed light can be use to explain the absorption enhancement due to Lambertian scattering. The authors were able to show that the fraction of reflected light leaving the boundary of a randomized surface can be given by:

$$f = \frac{\int_0^{\theta_c} B \cos\theta \sin\theta d\theta}{\int_0^{\pi/2} B \cos\theta \sin\theta d\theta} = \frac{1}{n^2} \quad (2.12)$$

where B is the internal brightness, assumed to be uniform and θ_c is the critical angle $\theta_c = \sin^{-1}(1/n)$. Furthermore, in an effort to sum up the path lengths of weakly absorbed light rays that leaves the front surface, they assumed a randomized surface at the top and a rear surface of reflectivity, R. This gives:

$$P = W[2(1 - R) + 4fR + 6R(1 - f)(1 - R) + 8f(1 - f)R^2 + \dots] \quad (2.13)$$

$$= 2W \left(\sum_{N=0}^{\infty} [(2N + 1)(1 - R) + (2N + 2)fR][R(1 - f)]^N \right)$$

where f is the fraction of the light escaping out at the top surface (transmittance).

Using power series Equation 2.13 becomes:

$$P = \frac{2W(1+R)}{[1-R(1-f)]} \quad (2.14)$$

When they set the values for f equal to $1/n^2$ and $R=1$ for the case of unit transmittance of top surface and a perfect back reflector, Equation 2.14 resulted in an average path length of

$$P = 4n^2W \quad (2.15)$$

where W is the thickness of the wafer and $4n^2$ is the absorption enhancement which is often known as Lambertian limit or Yablonovitch limit for weakly absorbed light.

Deckman *et al.* [96, 114] developed a more general expression for the limit of absorption enhancement for Lambertian scatterer. Their approach applies to both the intermediately absorbed light and weakly absorbed light. The expression for absorption is given by (supposing the dependant absorption in the contacts of the solar cell is neglected):

$$A = \frac{1 - e^{-4\alpha_a W}}{1 - e^{-4\alpha_a W} + \frac{e^{-4\alpha_a W}}{n^2}} \quad (2.16)$$

where α_a is the absorption coefficient.

2.5.3.2 Comparing Prior Results from Textures Simulation Using Path Length Enhancement

To investigate the path length enhancement of any texture using ray tracing technique, the light rays are considered to be weakly absorbed light. It is assumed that the rays do not get absorbed once they are coupled within the substrate but are redirected until they find their

way out of the substrate through the front surface. Also, the back surface is to be flat and acts as a perfect reflector as illustrated in Figure 2.7.

Campbell *et al* [8], used ray tracing to study the path length enhancement of different textures. They compared the number of rays remaining inside the substrate with the number of rays that passes through the cell. The Results are present in Figure 2.8. From the result present by Campbell *et al* [8] in Figure 2.8, the lambertain surface produced a high performance in trapping the rays for smaller number of passes than for large number of passes. The result also showed that the light trapping performance for the perpendicular slat is superior to that of the lambertian surface. It is also shown random pyramids perform quite close to the Lambertian.

In a similar work, Brendel *et al.* [115] used ray tracing to compare the effect of standard deviation in path length enhancement with the facet angle of different textures. Their study showed that virtually all the textures examined in the study attained the $4n^2$ limit (see Figure 2.9). They however concluded that the least standard deviation in path length enhancement was observed for the sharp prism groove at a facet angle of 17° .

2.5.3.3 Simulation results for Front Surface Reflectance Characterization from Prior work

The various textures compared in the preceding section have shown the textures have different capabilities to trap light rays within the substrate. Nevertheless, the path length enhancement of the textures alone is not adequate to ensure an efficient light management. One other task that can be performed by the textures is the effective coupling of light rays into the substrate. Since the different types of textures have different coupling capabilities, the best way to evaluate the light trapping effect is by comparing the front surface reflectance. A 2-D reflection distribution model was first presented by Rodriguez *et al.* [116]. They explained the construction of random pyramid texture. Later on, Baker-Finch *et al.*

[117] adopted the same model to study the reflection pattern of the textures for normally incident light. The authors chose the height of the starting pyramid to be between h_{\max} and h_{\min} and assumed that the light ray will initially strike this pyramid and then reflect towards a new pyramid in destination unit cell (Figure 2.10). This allows the light ray to propagate from one cell to a new cell until it can no longer be confined by the texture.

In addition, they used the concept of geometric optics to calculate the front surface reflectance and argued that the light rays that strikes on the regular upright and inverted pyramid texture follow preferential paths. They were able to use ray tracing and geometric optics show that the regular upright pyramidal rays follow two paths which they named *A* and *B*. They were able to established that, for all normally incident rays that intersect a pyramidal facet (following paths *A* and *B*), 88.9% of incident rays experience a secondary reflection, while the remaining 11.1% experience tertiary reflection. The total reflection was then calculated using the expression:

$$R_{reg,up} = 0.8889R_A + 0.1111R_B \quad (2.17)$$

where R_A and R_B represent the reflection of path *A* and *B* respectively.

For regular inverted pyramids, Baker-Finch *et al.* [117] obtained a similar expression that has three preferential paths *A*, *B*, and *C*. Of these three paths, two are the same as those for regular upright pyramid while the third path that bounces thrice before leaving the substrate (see Figure 2.11). The expression for the total reflection is given by:

$$R_{reg,inv} = 0.5789R_A + 0.0211R_B + 0.4R_C \quad (2.18)$$

With the above model and calculation, Baker-Finch *et al.* [117] have been able to create an open source program that can be used to analyze the front surface reflection of silicon solar cells. This is known as the OPAL software version 1 and 2. However, for the

random upright pyramids, Yun *et al.* [118] used a 3D ray tracing calculus to explain the reflection of the preferential paths. Unlike Baker-Finch *et al.* [117], an analytical model presented in chapter three is used to determine how incident light interacts with textured micro-pyramidal facets on alkali-textured silicon surfaces for a full range of incidence angle to the silicon substrate.

2.6 Theory

2.6.1 Determination of the Tilt Angle of the Pyramids: Vector Geometry Approach

Among the silicon wafers used in the silicon solar industry, (100)-oriented wafers are the most geometrically appealing since the orientations of {111} planes can be easily located on them [2]. During wet anisotropic etching, grooves with {111} sidewalls are exposed by KOH solution [25] and are aligned with {100} planes at specific angles [8]. This is attributed to its high anisotropy against {111} planes [6, 199]. However, to understand the etching behaviour of the (100)-oriented wafers, it is important to know the relative positions of different crystal planes in these wafers and the angles that they make with each other, after etching. In order to achieve this, the angles between the individual crystallographic planes can be calculated using vector operations (dot products), since the angle between {100} and {111} planes are the same as the angles between the unit vectors of their normals. Thus, by inspection, the unit normals of both the (100) plane and the (111) plane can be obtained from their Miller indices, as shown in Figure 2.12.

In order to demonstrate the geometrical properties of silicon crystal on a (100) plane, the dot product is then used to obtain the angle (tilt angle) between the (111) plane indices and the (100) plane indices as follows:

$$\hat{n}_{100} \cdot \hat{n}_{111} = |\hat{n}_{100}| |\hat{n}_{111}| \cos \theta. \quad (2.19)$$

$$\cos \theta = \frac{[1,0,0] \cdot [1,1,1]}{|100| |111|}$$

$$\cos \theta = \frac{1+0+0}{\sqrt{1} \sqrt{3}}$$

$$\theta = \cos^{-1} \left(\frac{1}{\sqrt{3}} \right)$$

$$\theta = 54.74^\circ$$

where $|\hat{n}_{100}|$ and $|\hat{n}_{111}|$ represent the magnitudes of the unit normal vectors and θ is the angle between the (111) facet and the (100) substrate.

The above angle corresponds to that specified from Wulff's stereographic projections of a (100)-oriented silicon crystal [120]. Due to symmetry of the (111) anplane on the (100) plane, the (111) plane also meets the (010) plane and the (001) plane at an angle of 54.74° . The intersection of the (111) plane also forms a square-based pyramid. This implies that, for all incident light rays normal to the substrate, the primary reflections are oriented at 54.74° to the substrate surfaces. However, for actual industrial c-Si solar cells, where non-ideal etching is observed, a slightly smaller base angle (or facet tilt angle) is normally observed [66, 67]. This has been shown to be less than 52° in Refs [66, 67].

2.6.2 Determination of the Heights of the Pyramids

As previously discussed, the anisotropic etching of (100)-oriented wafers produces squared-based pyramidal structures that are defined by four (111) planes located on (100) plane. A 2D model of an ideal pyramid on (100)-oriented wafer is illustrated schematically in Figure 2.13. The Atomic Force Microscopy and Scanning Electron Microscopy are often used to reveal and estimate the base length of the pyramids. This can be used to estimate the height of the pyramids theoretically.

Due to symmetry of the (111) plane on the (100) plane, we can consider half of the idealized pyramid in Figure 2.13 to estimate the height of the pyramid. As illustrated on the left part of Figure 3.7, the base and the side length of the pyramid represents the (100) and

(111) planes respectively. While the tilt angle (the angle between the (111) and (100) planes) is given as 54.74° for an ideal case. Using this information, the height of the pyramid can be calculated using the relation:

$$\tan \theta = \frac{h}{a} \quad (2.20)$$

$$h = a \tan(54.74) \quad (2.21)$$

As an example, consider the case of a base length, B , obtained from an AFM image to be $1 \mu\text{m}$. Equation 2.21 can be used to obtain the height of the pyramid as follow:

$$h = 1 \tan(54.74)$$

$$h = 1.4 \mu\text{m}$$

Also, the side length of the pyramid can be calculated using the following expression:

$$L = \frac{1}{\cos(54.7)} \quad (2.22)$$

$$L = 1.72 \mu\text{m}$$

However, for a more complicated case where the height of several hundred pyramids is to be determined, special programs [121] are required. One of such programs has been developed by *Kuchler* et al. [121]. They combined two REM pictures of textured silicon wafers taken at asymmetrical angles (for example 10° and -10° , symmetrical pictures) and then by using the stereoscopic technique (also known as machine vision) to reproduce the pyramidal texture via simulation. They were able to determine the pyramid sizes of over 1500 pyramids using this technique.

2.7 Fatigue in Silicon MEMS Structures

In recent years, an enormous collection of MEMS applications (inertial sensors, ink jet cartridge nozzles *etc.*) have emerged [122-123]. This has led to the introduction of a variety of commercial products (medical and computer devices) into the marketplace. The suitability and success of silicon material in micromachining technology have made it a regular choice for most MEMS applications [125]. However, the reliability of these devices is dependent on the type of loading and environmental conditions.

Consequently, the performance and reliability of MEMS structures are frequently affected by cyclic loading and the environment. In particular, the materials used for the safety-critical applications are often subjected to aggressive mechanical and chemical environments. The engineering design of reliability, therefore, requires models that account for the time- and cycle-dependent degradation of MEMS materials. However, most MEMS materials undergo failure when subjected to cyclic stresses. This occurs due to a phenomenon known as “*fatigue*”.

In general, there are two accepted types of mechanisms of fatigue associated with fracture process: ductile and brittle. The ductile mechanism on one side is usually attributed to the metallic materials and is supplemented by the cyclic accumulation of plastic deformation through the generation and motion of dislocations. In this case, failure is as a result of the crack nucleation and its crack propagation, either pre-existing or created by alternately blunting and sharpening the crack tip.

Conversely, brittle materials such as single-crystal silicon demonstrate very low dislocation mobility at ambient temperatures as a result of high Peierls forces. This implies that if fatigue occurs in these materials, then the primarily different mechanism for dislocations is not involved. In reality, the fatigue in some polycrystalline ceramics and ordered intermetallic compounds [126, 127] is governed by kinematically irreversible deformations through the crack-tip shielding mechanisms. This leads to cycle dependent

degradation of the toughness of the material. However, covalently bonded diamond structures like single-crystal silicon do not demonstrate any degree of shielding to degrade. Therefore, the crack-tip shielding mechanisms would not be expected in these materials.

Moreover, it has been established both experimentally [13, 128–131] and theoretically [132] that bulk single-crystal silicon is safe from both cyclic fatigue and environmentally assisted cracking such as the stress – corrosion cracking [13, 15, 130, 133–135]. However, such protection from long-lifetime degradation can be beneficial in applications such as sensor technology and solar panels where periodic mechanical, electrical, or thermal stresses operate [129].

As a result of the aforementioned reasons, fatigue of silicon was not expected when Connally and Brown in 1992 [125] revealed that a silicon specimen of micrometer-size dimensions prematurely failed under cyclic fatigue loading in room-temperature air. Their findings have been validated by many other studies in the last decade [10, 18, 128]. More recently, different research groups have examined and reported on the experimental and analytical/computational studies of the fatigue behaviour of both single crystal [137] and polycrystalline silicon [138].

Since silicon thin film is one of the most common materials in micro-electro-mechanical systems to date, it is of extreme importance to understand the silicon fatigue mechanism in order to be able to control the fatigue damage in silicon-based MEMS devices. Despite the extensive research on the design and characterization of various properties of MEMS structures, there is still no consensus on the mechanism of fatigue in silicon MEMS structures [139].

2.7.1 Single-Crystal Silicon

Prior work has shown that when fatigue in silicon occurs at high enough stress amplitudes, cracks are initiated and grow through the material before the eventual failure of

the silicon structure. In the pioneering work on fatigue of Si MEMS structures, Connally and Brown [125] used a notched, electrostatically actuated resonator system (Figure 2.15) with a resonance frequency of 12 kHz and a stress ratio of -1, and demonstrated that fatigue was caused by slow crack growth that occurred by environmental-assisted cracking in the silica layer that forms on silicon upon exposure to oxygen. They obtained stress-life and fatigue crack growth rate data that suggested a strong influence of water vapour on the fatigue of silicon. Furthermore, they proposed, in particular, that the fatigue-crack growth rates are rate-limited by the reaction rates at the crack tip or by transport of reaction species to, or from, the crack-tip region [140].

In summary of their work, Connally and Brown concluded that the actual mechanism governing crack growth in micron-scale silicon devices is more complex than simple environmentally-assisted fatigue of silica, although water, indeed, accelerates or initiates crack propagation.

Subsequently, Tsuchiya *et al.* [141] verified the effect of environment on the fatigue behaviour in silicon single-crystal silicon films. Like Connally and Brown, they used silicon specimens fabricated by silicon micromachining technology. As stated by Tsuchiya *et al.* [141], the fatigue damage increases with increasing fatigue life, although no precise evidence of this damage were provided. They also established that cycling in dry air leads to more cycles than cycling in humid air. Fatigue failure in air was observed after 2.9×10^7 cycles for a specimen initially loaded at a stress 10% lower than the cyclically measured fracture strength and 20% lower for a specimen run for 1.6×10^8 cycles. This demonstrates that testing environment highly affects both the specimen's fracture strength and fatigue life. However, the authors attributed their findings to a mechanism involving oxidation at a crack initiation site on the silicon surface that allowed additional crack growth. These results have been validated in recent works by Koskenvuori *et al.* [142] and Pierron *et al.* [143]. They

both provided additional evidences that silicon films exhibits an increasingly significant degradation over time in air than in vacuum [142, 143].

For fracture surface examination, scanning electron microscopy (SEM) and atomic force microscopy (AFM) are used to acquire information about the crack initiation and failure mechanisms [20, 144-146]. Moreover, it has been shown that there is no evident fracture initiation region in specimens with short lives and those specimens contain features that are commonly observed on brittle material fracture surfaces. Furthermore, it has been established that the failure in a short-life specimen evolves by cracks on multiple $\{111\}$ planes with final failure taking place by cleavage on a (111) plane, after combining the multiple crack fronts [138, 147, 148]. Cleavage steps, formed on the $\{111\}$ fracture surfaces as a way of dissipating energy, were addressed by Muhlstein *et al.* [147] with regard to perturbations in the applied loads, obstacles in the crack path, bifurcation of fast-running cracks, and the coalescence of micro-cracks.

Conversely, for the long-life fracture surfaces, the initiation region can be clearly detected and it is located near the surface of the notch. Here, the fracture surface is smooth and does not contain any steps like that of the short-life. The fracture proceeds predominantly along $\{110\}$ and suggests that the active cracking mechanism under cyclic fatigue loading is different from that seen during quasi-static overload failure [147]. However, Sundurarajan and Bhushan [149] obtained SEM images that reveal a high-energy fracture on a $\{100\}$ plane in combination with low-energy cleavage on $\{111\}$ planes. The fracture surfaces were found to be smooth, without facets or irregularities. The authors suggested that fatigue mechanism similar to environmentally assisted cracking are experienced when fracture occurs by low-energy cleavage on the $\{111\}$ planes.

Furthermore, the method of loading affects the growth of a subcritical crack. For instance, in monotonic loading a discrete step-like crack growth process is observed [131, 150] (Figure 2.16). The increase of the load leads to the unstable fracture mode when the

stress intensity, K_I , approaches the toughness of the material. However, K_I can decrease with crack extension leading to the crack arrest depending on the geometry of the specimen [131, 150]. The experimental studies for constant-load mode show that subcritical cracking occurs only for $0.9 K_{Ic} < K_I < 0.98 K_{Ic}$, where K_{Ic} is the toughness of the material (Figure 2.17). This implies that the subcritical crack growth occurs in the region III in v - K_I curves (v is the crack growth rate given by $v = CK^n$, where C and n are constants, and n is higher than 100.) where the crack velocity outperform transport of the environmental species. As a result of this, it has been established that environmentally-assisted subcritical cracking is absent in monotonically loaded micron-scale silicon [131, 150].

For cyclically loaded specimens the crack-growth behaviour is observed to be step-like in nature, with unstable crack extension when the maximum applied stress intensity reached the fracture toughness [131, 150]. However, under decreasing K conditions, cracks were observed to arrest. The resulting growth rate versus K_{max} curves were similar to the curves obtained under monotonic loading, which suggested that the relevant crack-growth process in single-crystal silicon was not true cyclic fatigue. This conclusion was further supported by the fact that fracture surfaces under cyclic and monotonic loading were similar. The authors also suggested that fatigue mechanisms involving cracking of a surface reaction-layer could be a viable mechanism.

2.7.2 Polycrystalline silicon

Like single-crystal silicon films, experimental studies from prior works has shown that material failure in polycrystalline silicon specimens is influenced by factors such as loading conditions, operating frequency, and majorly, environment [144-146]. In an early work by Van Arsdell and Brown [151] on the fatigue in polycrystalline silicon films, the change in resonant frequency of a pre-cracked polysilicon device under fatigue loading in wet air was reported. The authors observed that the resonant frequency of the device decreased

when it was fatigued in humid air (50% or 75% relative humidity, 30°C), but remained unchanged when it was fatigued in dry air. They interpreted the results as subcritical crack growth through environmentally assisted cracking mechanism. Based on the transgranular crack path shown by fracture surface investigation done by Van Arsdell and Brown [151], the environmentally assisted cracking was suggested to involve the native oxide film rather than the polysilicon itself. They further claimed that this mechanism known as “static fatigue” would facilitate additional oxide growth at the crack tip and that it includes only effects of the environment and stress level, but claims the fatigue behaviour is independent of the number of load cycles.

Using the same devices as those used by Van Arsdell and Brown [151], Muhlstein *et al.* [10, 18, 19, 138, 152–154] measured the thickness of the surface silica layers on the specimens using transmission electron microscopy (TEM). From their study, they observed that the surface oxide thicknesses after fatigue cycling to failure were three times greater in highly stressed regions than in the non-stressed regions without the occurrence of heat (Figure 2.18). This validated the work by Van Arsdell and Brown [151]. Muhlstein *et al.* [10, 18, 19, 138, 152–154] also reported TEM studies of one specimen that was cyclically stressed but not to failure. The results showed several stable small cracks within the thickened surface oxide layer, indicating the presence of subcritical crack growth.

Furthermore, it has been shown that the specimens that are treated with a self-assembled monolayer (SAM) coating during fabrication (surface oxide formation prevention) experience smaller dependence of lifetime on the peak stress amplitude. Based on this assumption, Alsem *et al.* established that the absence of oxygen and water vapour in a 2×10^5 Pa vacuum environment completely suppressed the occurrence of delayed fatigue [140]. They also showed that samples tested in high relative humidity air ($> 95\%$ RH, 30°C) failed after fewer numbers of cycles than corresponding samples tested in ambient air ($\sim 35\%$ RH,

25°C). With the insights from these studies, the fatigue of silicon thin films was attributed to a mechanism of sequential, cyclic stress-assisted oxidation and environmentally assisted cracking of the surface oxide layer which forms upon exposure to moisture- and/or oxygen-containing atmospheres, a mechanism that they termed “*reaction-layer fatigue*” [140].

In an effort to support the reaction-layer model Muhlstein *et al.* [19, 152] performed a finite-element modelling that claimed a decrease in natural frequency of the fatigue characterization structure evolution in the form of oxide thickening (-0.5 Hz per nm of oxide growth) and subcritical crack growth (-1 Hz per nm of crack extension) within the oxide (Figure 2.19). The result of the calculated crack size was close to the maximum crack extension observed experimentally. Since the crack size is less than the surface oxide layer, the entire process of fatigue crack initiation, growth, and the onset of final failure of the entire structure occurred within the oxide layer [155]. Following these observations and the fact that a crack in the oxide layer must cause failure of the entire structure, the criterion for this mechanism was proposed, which says that the thickness of the oxide layer, h , must be greater than or equal to the critical crack size, a_c , to fail the entire structure (*i.e.*, when $a_c < h$).

Pierron and Muhlstein [156] further expanded this numerical model to account for a different failure scenario where stable crack growth in the oxide now becomes unstable crack growth when the crack gets to the silicon/oxide interface (*i.e.*, when $a_c = h$; this lowered the oxide thickness that is potentially susceptible to reaction-layer fatigue to ~15 nm, compared to ~50 nm required in the previous model). The mechanism also explained the decreasing growth rates observed for cracks propagating within the oxide layer [155].

Another mechanism, complementary to reaction-layer fatigue, was proposed based on the surface topology changes with increasing distance from the notch seen in *in situ* AFM images of the region near the notch (Figure 2.20), before and after cyclic actuation [20, 144, 145, 157, 158]. These changes indicated a role of stress in the evolution of surface topography under cyclic loading and were ascribed to the roughening of the surface oxide

layer (Figure 2.20), which in turn was associated with a mechanism of cyclic stress-assisted dissolution of the surface oxide layer such that deep grooves are formed where the dissolution is fastest that could result in fatigue crack nucleation (Figure 2.21). One drawback of this model as stated by Kahn *et al.* [159] is that cyclic stress-enhanced oxidation has never previously been observed. Although Allameh *et al.* [144, 145] reported that their specimens had an initial surface oxide of 2 – 4 nm. They used the same structures as Muhlstein *et al.* [19], who showed surface oxides of about 30 nm. Another concern is that Allameh *et al.* [20, 144, 145, 157, 158] used the model based on the stress-dependent surface reaction model of Yu and Suo [160], which considered monotonic stresses rather than the cyclic stresses that Allameh *et al.* used exclusively.

Kahn *et al.* [128, 161 – 164] suggested a completely different mechanism for the fatigue of micron-scale polysilicon based on results obtained from specimens tested at varying stress ratios ($-3 < R, 0.5$) in laboratory air and in a medium vacuum (8 Pa pressure). The first claim by Kahn *et al.* is that fatigue crack initiation and growth occurred during cyclic loading in both air and vacuum, although the process was faster in air. The authors then suggested a purely mechanical mechanism for the fatigue behaviour of silicon thin films via subcritical cracking of the silicon itself. Furthermore, their findings show that the low-cycle fatigue strength of the electrostatically actuated single edge notched micro-specimens was affected more by the stress ratio than by the environment. On the basis of this, they concluded that the fatigue mechanism for silicon thin films was strongly affected by the compressive portion of the loading cycle. The authors think this could create a micro-crack at the surface due to wedging on surface asperities and thus allow further crack growth as a result of a mechanism similar to far-field cyclic compression fatigue of brittle ceramics. The investigations of the authors on high-cycle ($10^4 - 3 \times 10^8$ cycles) fatigue behaviour in air and vacuum found no fatigue failures in a medium vacuum. This allowed Kahn *et al.* [159] to

propose that thickened surface oxide on newly formed crack surfaces in air could cause wedging effects that would create additional subcritical cracking or that wear debris formed in vacuum could prevent crack closure and therefore decrease crack driving force and growth [159].

However, the finite-element modelling used in fracture mechanics for the calculations of the crack-opening profile and the driving force for advance of wedged cracks showed that, in compression, such wedges do not cause an increase of the magnitude of the stress-intensity factor. This implies that this mechanism cannot contribute significantly to the fatigue of silicon thin films [140]. Subsequently in their experiments on mean stress effect on the low-cycle fatigue of Pd-coated undoped and B-doped polysilicon film, Kahn *et al.* [165] found that increasing the amplitude of the cyclic stress with a positive mean stress led to the higher fracture stress, whereas negative mean stress led to the lower fracture stress.

To account for all their observations Kahn *et al.* suggested three possible fatigue mechanisms. The first of these was based on the idea of the micro-cracking of the silicon and was discarded later as inappropriate as an explanation of the weakening and the strengthening due to crack tip shielding. A second mechanism was suggested involving dislocation activity, which would cause crack-tip blunting in the case of a strengthening effect and crack-tip blunting followed by sharpening for a weakening effect. The third proposed mechanism involved grain-boundary plasticity, where an amorphous grain-boundary region hitting the surface under stress would experience a nonconventional plastic deformation in shear, which would then cause a residual compressive stress, possibly resulting in the observed strengthening effect. To support this model Kahn *et al.* presented results of their element modeling, where they showed that with such grain-boundary plasticity residual compressive stresses could occur. However, as argued by Alsem *et al.* [140], there is no experimental evidence for these simulated results; furthermore, the fact that single-crystal micron-scale

silicon is also susceptible to fatigue failure is totally inconsistent with any mechanism involving only grain boundaries.

Bagdahn and co-workers [166-168] combined their data on the influence of frequency on the high-cycle fatigue behaviour with those of Muhlstein *et al.*, Kahn *et al.*, and Kapels *et al.* into a single plot of normalized peak stress versus fatigue lifetime and found that all the data followed the same curve (Figure 2.22). They concluded that fatigue lifetime depends only on the number of cycles, not on the total time or the frequency of the test, and fit the results to the equation:

$$\frac{\sigma_f}{\sigma_c} = N_f^{-0.02} \quad (2.22)$$

where σ_f is the peak stress in the fatigue cycle, σ_c is the monotonic strength, and N_f is the number of cycles to failure. They also noted an increase in surface roughness of the top surface of their specimens in the vicinity of the fatigue fracture [168]. Finally, they concluded that there should be an additional effect (other than the environmental influences) to account for all the results.

2.7.3 Mechanisms of Fatigue in Silicon MEMS Structures

From the qualitative results obtained by Muhlstein *et al.* [18, 19], it is possible that the source of fatigue in single crystal silicon is similar to that of polysilicon materials. Also, the study by Bagdahn and Sharpe [168] has shown that undoped polysilicon with a 2 nm surface oxide and a sputtered Pd film behaves the same under cyclic loading as P-doped polysilicon with a 30 nm surface oxide. Hence, it is reasonable to expect that any proposed fatigue mechanism for silicon must explain all of the observed phenomena. These phenomena include: an increase in high-cycle fatigue lifetime with a decrease in peak stress, a decrease in the resonant frequency of specimens during a fatigue test, a decrease in low-cycle fatigue strength with decreasing stress ratios, R , an increase in fracture- producing flaw size with

decreasing fatigue strength, no dependence on testing ambient for low cycle fatigue, dependence on ambient for high-cycle fatigue, and morphological changes including an apparent oxide thickness increase and surface roughness increase in the area of high stress. However, three mechanisms have been proposed: stress-assisted surface oxide dissolution by Allameh *et al.* [144, 145], reaction-layer fatigue by Muhlstein *et al.* [19], and mechanically induced subcritical cracking by Kahn *et al.* [164].

The stress-assisted surface oxide dissolution model [144, 145] involves cyclic stress enhanced oxidation, followed by uneven “dissolution” of the surface oxide such that deep grooves are formed where the dissolution is fastest; these grooves are then sites for crack nucleation. Allameh and co-workers [20, 144 - 146] used only AFM to investigate their devices, and inferred the oxide thicknesses from the AFM results. Still, to achieve the deep grooves reported by Allameh *et al.*, oxide growth, oxide redistribution, or some other mechanism of morphological change must have occurred.

The reaction-layer fatigue model [19] also involves cyclic stress enhanced surface oxide thickening, which then undergoes environmentally assisted stress corrosion cracking. The process reoccurs until a critical crack size is attained, and then the silicon itself fractures catastrophically. Specifically, the fatigue damage occurs only in the surface oxide, while stress corrosion is dependent on time and monotonic stress. However, Kahn *et al.* [159] argued that the TEM, which was used by Muhlstein *et al.* [19] to obtain the experimental results used to support this model, is both unconventional and quite difficult to use to determine the thickness of a surface layer on a sidewall. This is based on the fact that the micro-fabricated sidewalls of the polysilicon specimens are neither perfectly flat nor perfectly vertical. Furthermore, they claimed that this type of analysis cannot determine whether the thickness of the surface oxide is uniform through the 2000-nm height of the polysilicon device, or whether the observed thickness increase is due to redistribution of the initial oxide [159]. Finally, Kahn *et al.* considered another concern about the SAM-coated results, which

showed failures at 10^7 and 10^8 cycles (4.2 and 42 min) for specimens with peak stresses of 2.8 GPa. For these devices to fail via the reaction-layer mechanism the SAM must first break down, then a surface oxide of sufficient thickness (20 nm) must grow, followed by stress corrosion cracking of the oxide layer, all within the time span of a few minutes.

The mechanically induced subcritical cracking model states that subcritical cracking occurs in the silicon itself when subjected to cyclic loads, particularly cyclic loads with large compressive components [164]. Fatigue damage of bulk brittle materials under cyclic compression has been well established [169]. Thus, this model explains the fatigue results that depend on stress levels but not on ambient, while the models that involve surface oxide growth better explain the fatigue results that have an ambient dependence. To explain the ambient effects on high-cycle fatigue, Kahn *et al.* [169] proposed that in air, surface oxide formation on mechanically induced subcritical cracks caused wedging effects that increased the applied stress intensity at the crack tips. There is another explanation for enhanced fatigue behaviour in humidity that does not involve chemical reactions with the environment. Increasing the relative humidity in operating air greatly reduces the amount of wear debris formed by contacting polysilicon components [170].

In fatigue of bulk ceramics, wear debris decreases crack growth by preventing crack closure and reducing the effective driving force for crack advance [171]. Similar wear debris formed in dry air or in vacuum could reduce the fatigue effects in polysilicon operated in these ambients. Therefore, the only feature of fatigue behavior not accounted for by this model is the surface roughness increase reported by Allameh and co-workers [144, 145] and Bagdahn and Sharpe [168]. It is possible that this phenomenon is restricted to silicon specimens with thick (30 nm) surface oxides, such as those used by these researchers, and that it is not a general feature of silicon fatigue.

2.7.4 MEMS Testing Techniques

Silicon specimens used in fatigue experiments are invariably fabricated using silicon micromachining techniques that utilize silicon wafers as substrates. This technology allows two types of loading: external and integrated. The external loading involves connecting the microfabricated specimens to a separate system that is used to apply forces. One simple external loading device is a nanoindenter. The tip of the nanoindenter is pushed downward on silicon cantilever beams [137, 148] or clamped–clamped silicon beams [172], to generate bending stresses. A similar technique used a lateral-motion load cell to push on the end of a beam attached to both a torsional bar and a tensile bar, to create tensile stresses in the area of interest [173]. Another external loading technique used a piezoelectric-based load cell to pull on silicon tensile specimens [166 - 168]. Finally, the silicon substrate can be attached to a piezoelectric shaker; when this actuator vibrates at the resonance frequency of the silicon device, the device will experience large amplitudes of deflection and high stresses [141].

Since the silicon specimens are fabricated on silicon substrates, it is possible to integrate the specimens with wafer-level micro-actuators that can generate the fatigue stresses using only electrical connections. Most of these micro-actuators use electrostatic forces, created with applied voltages. Both comb-drive actuators (actuators that involve the capacitance increase that results from the increased overlap of two opposing sets of long straight fingers) [17-19, 138, 144-146, 151-153, 157, 161-163] and parallel-plate actuators [175, 176] have been used. Another integrated microactuator exploits the thermal expansion of current-induced locally heated silicon to generate the fatigue stresses [17].

In general, the use of external actuation makes the silicon specimen fabrication much simpler, since the integrated micro-actuator is absent. However, the problems of attachment and alignment of external loading sources cause these experimental procedures to be cumbersome. For fatigue testing, it is advantageous to stress at relatively high frequencies. This is possible using external piezoelectric-based actuators, and especially for integrated

electrostatic actuation. Thermally induced loading suffers from long cooling times, which limit its testing frequencies to about 1 Hz [17]. As discussed above, it is also desirable that the loading system be able to apply monotonic as well as cyclic loads, be able to measure the monotonic strength of the specimens, and be able to test the specimens for long-term durability under constant stresses. Since the external loading schemes are relatively large, they all display this capability, except for the shaking technique.

For the integrated micro-actuators, the thermally induced stresses are large enough to test the monotonic strength, but the thermal stability of the device may not be high enough for long-term testing under constant loads. Electrostatic actuators typically do not generate sufficient force to study monotonic fracture. However, electrostatic comb-drive actuators can be made with enough comb fingers to cause both monotonic fracture at stress concentrations, as well as fatigue-induced fracture [162-164]. The disadvantage is that the device is relatively very large (about 2 mm × 2 mm), which decreases the yield of useful devices on a wafer processed in a semiconductor “foundry.”

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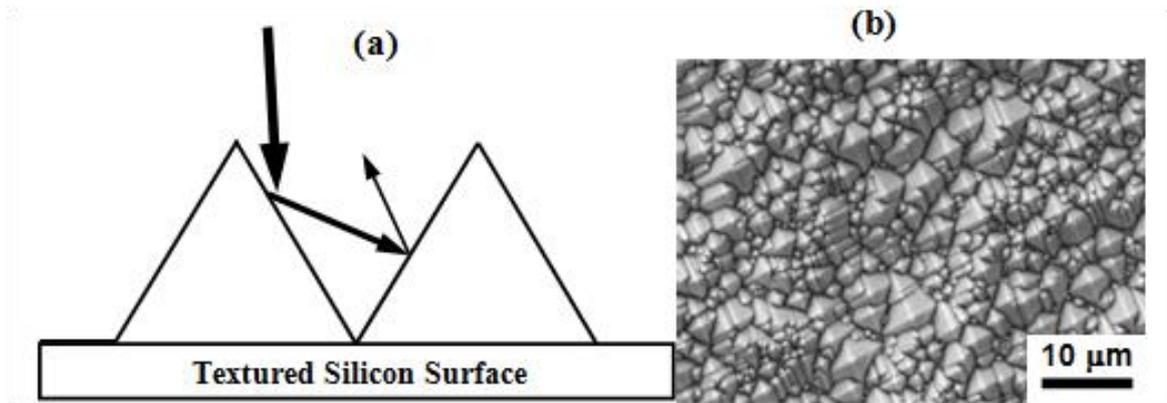


Figure 2.1: (a) Schematic of Light Interactions with Silicon Surfaces: Minimizing Reflection Loss on Textured Silicon Surface; (b) SEM image of Textured Silicon Surface.

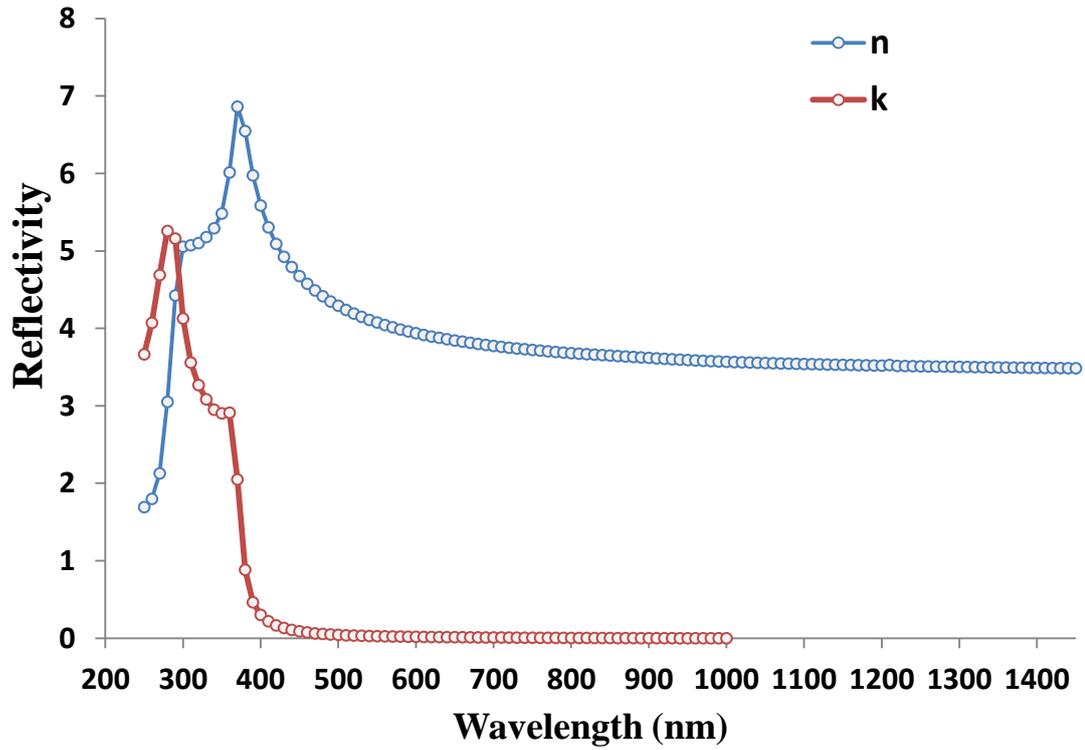


Figure 2.2: Real and Imaginary Parts of the Refractive Index of Silicon. Taken from Ref.

[27]

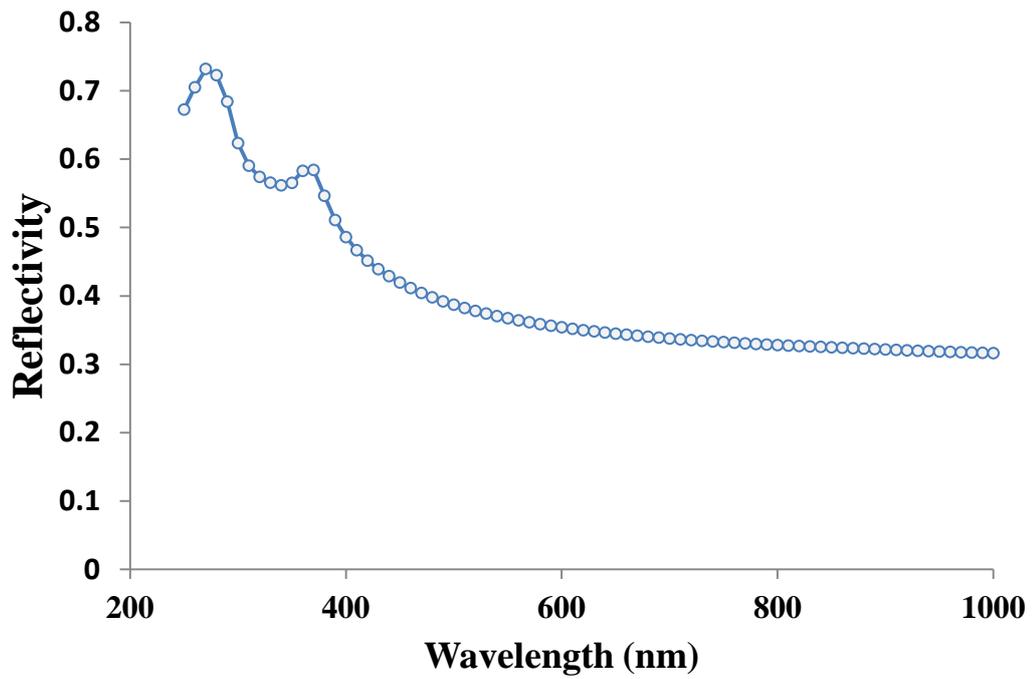


Figure 2.3: Reflectivity of Bare Silicon related to Normal Incidence. Taken from Ref. [27]

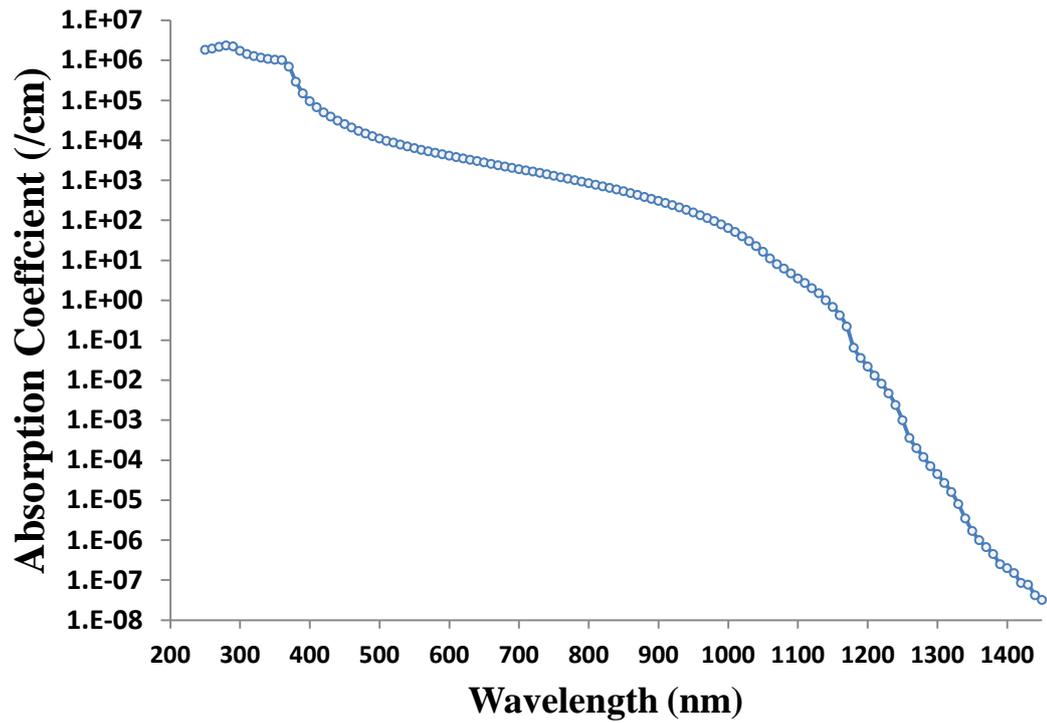


Figure 2.4: Absorption Coefficient of Silicon. Taken from Ref. [27]

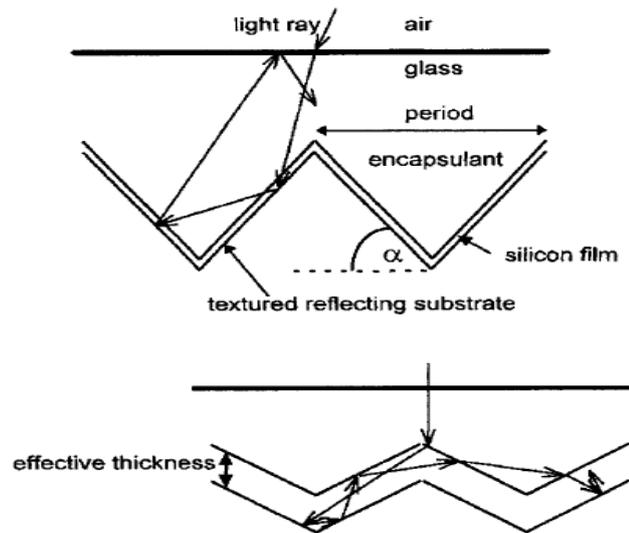


Figure 2.5: Examples of Structured Surfaces to Implement Light Trapping in Silicon Solar Cells. Taken from Ref. [102]

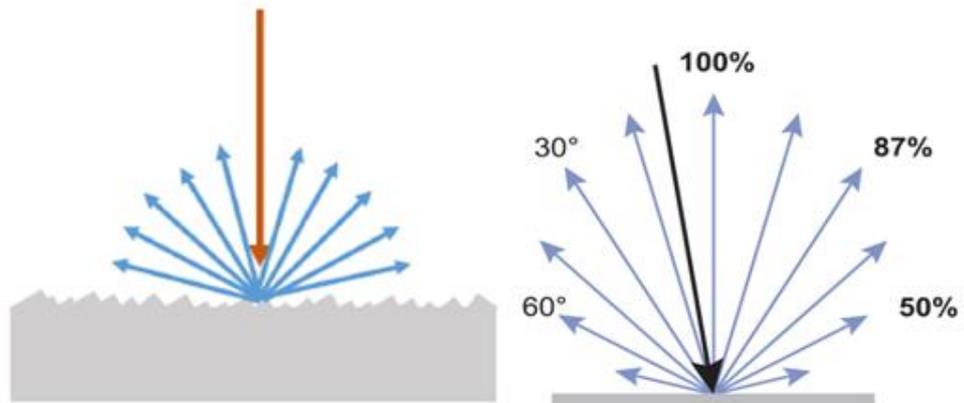


Figure 2.6: Lambertian Surfaces.

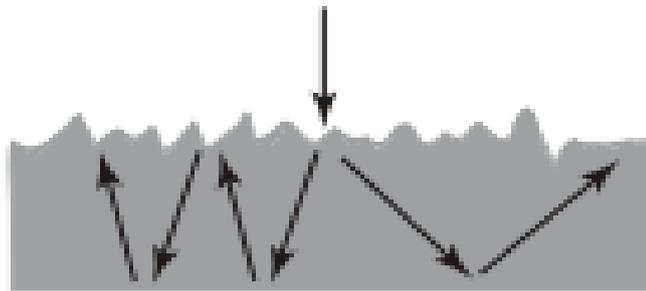


Figure 2.7: The Setup for Path Length Enhancement Simulations.

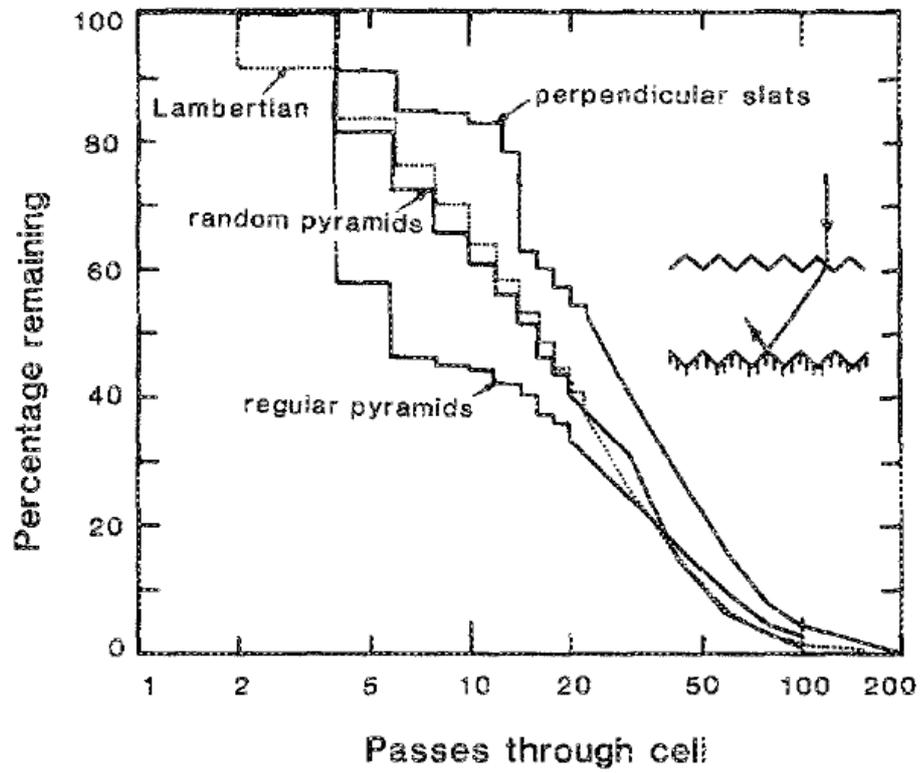


Figure 2.8: Percentage of Rays Remaining Versus The Passes Through Cell [8].

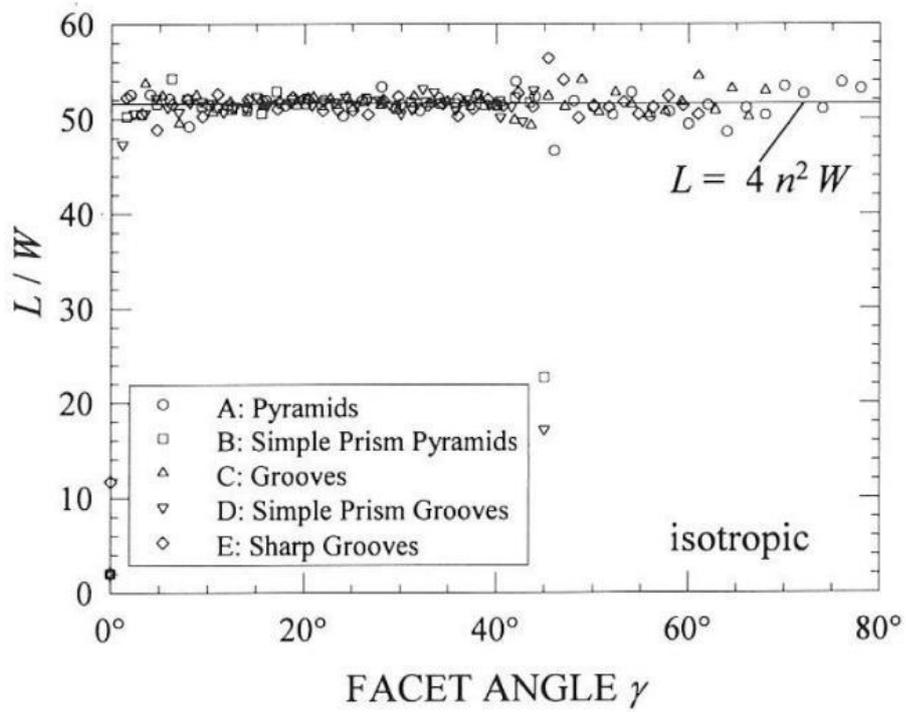


Figure 2.9: Path Length Enhancement versus Facet Angle [115].

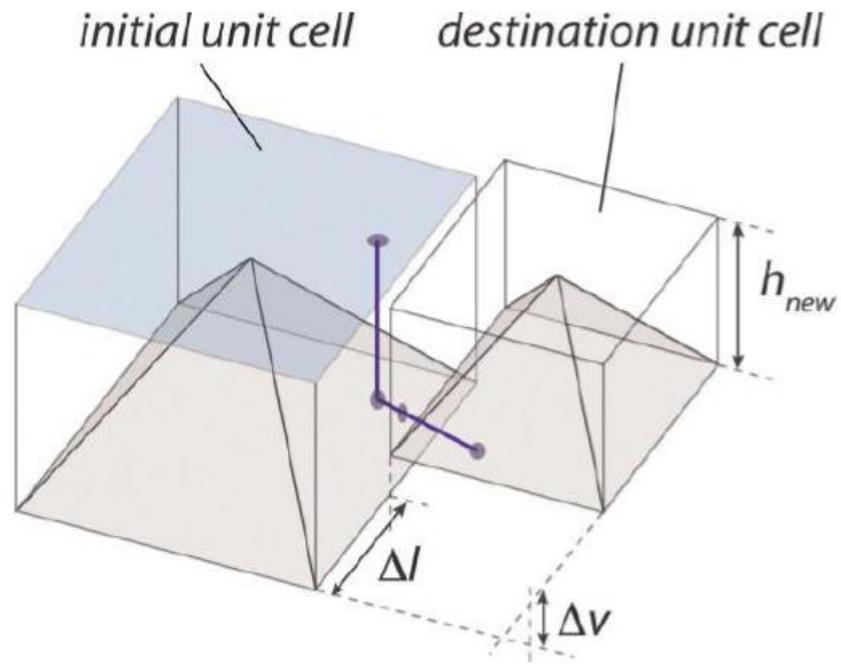


Figure 2.10: Random Upright Pyramidal Texture Creation. The Starting Unit Cell and Destination Unit Cell that has Random Height and is Laterally and Vertically Displaced Randomly with Respect to the Previous Cell. Taken from [117]

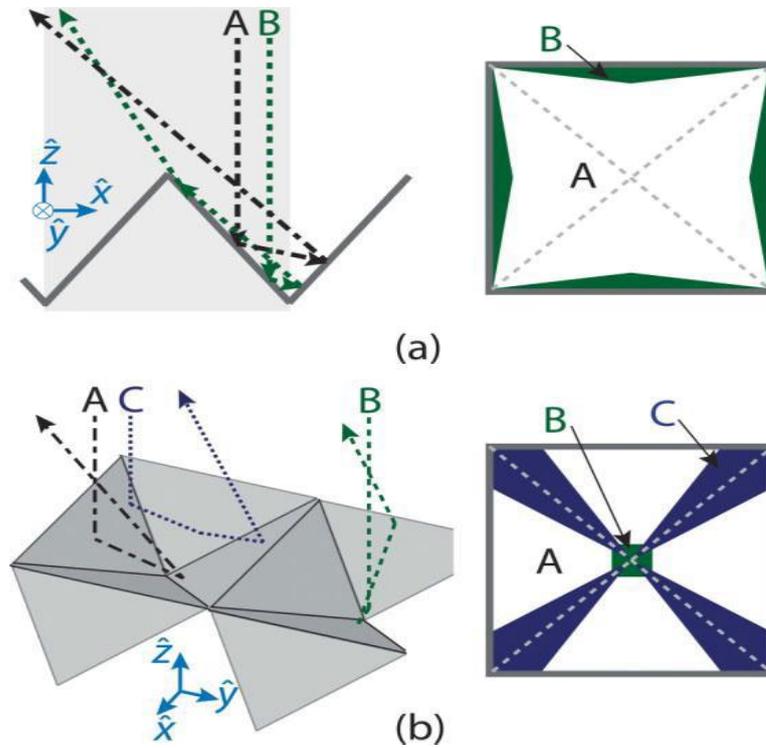


Figure 2.11: (a) Shows the Preferential Paths for Regular Upright Pyramids (B) Shows the Preferential Paths for Regular Inverted Pyramids. Taken from Ref. [16]

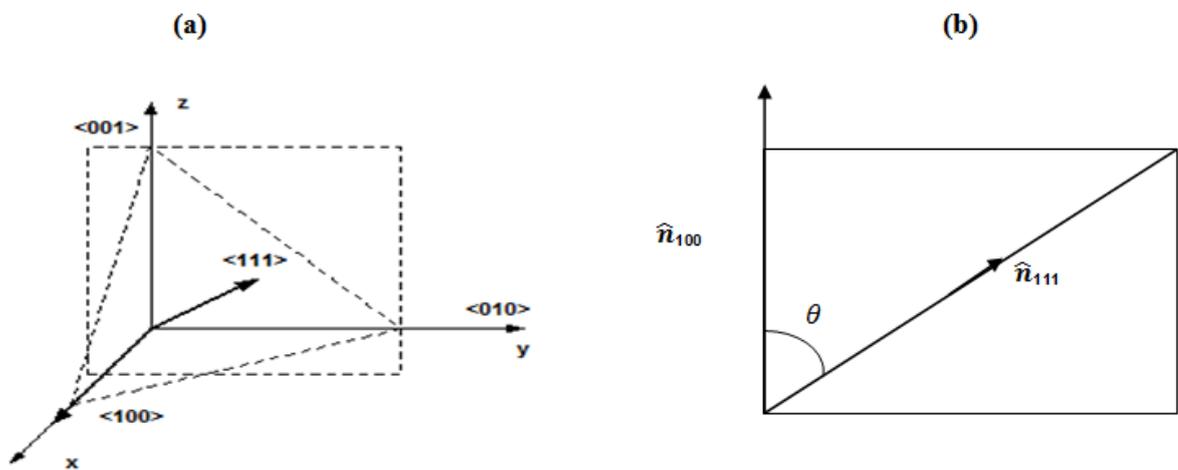


Figure 2.12: (a) the square and triangular shapes represents the (100) plane and (111) plane respectively (b) a rectangle including the main diagonal of the cube used to determine the angle of interest.

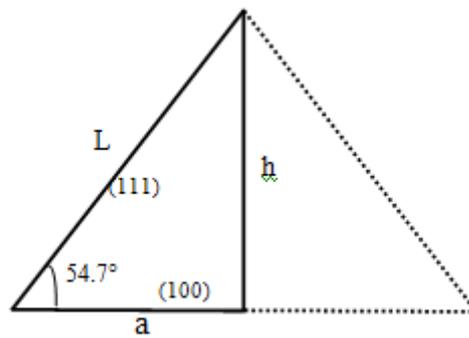


Figure 2.13: Schematic diagram of a 2D idealized pyramid formed on a textured (100)-oriented Silicon wafer.

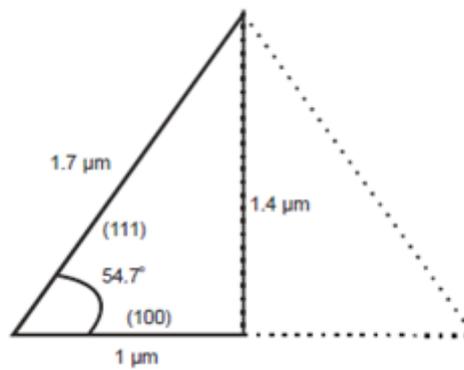


Figure 2.14: Calculated height of a 2D idealized pyramid.

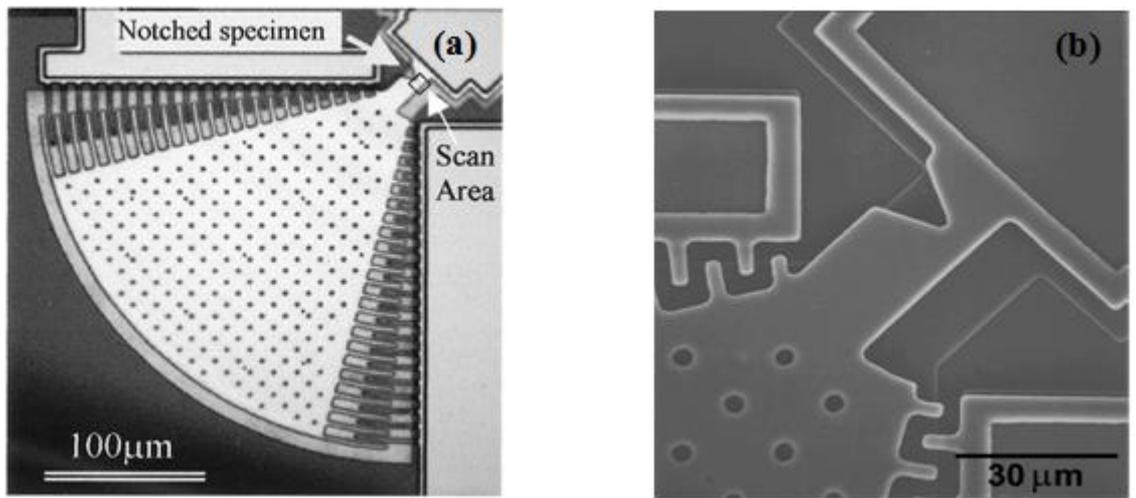


Figure 2.15: Scanning electron micrographs of resonator stress-life fatigue characterization structure. (a) The electrostatic comb drive actuator and notched cantilever-beam specimen, (b) an overview of the scan area on the left [146]

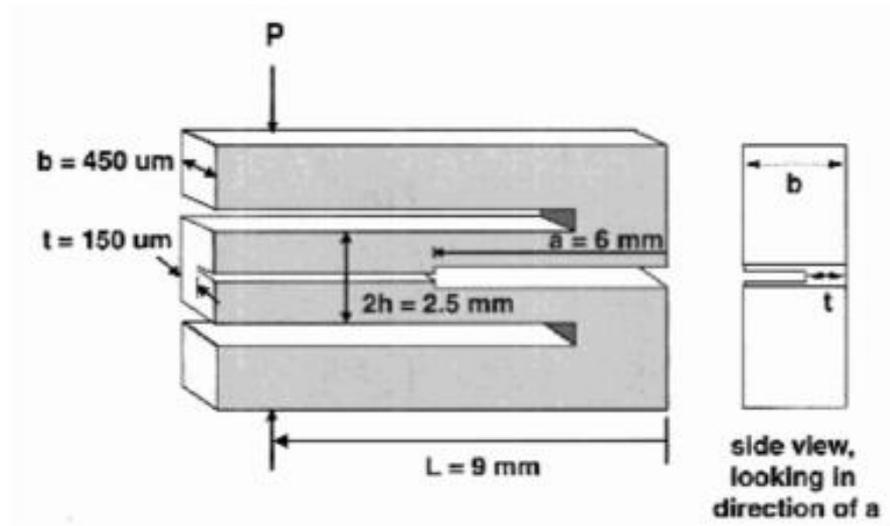


Figure 2.16: Schematic illustration of the compression-loaded double cantilever beam specimen. Specimen height is 7.6 mm with a length of 12 mm. [150]

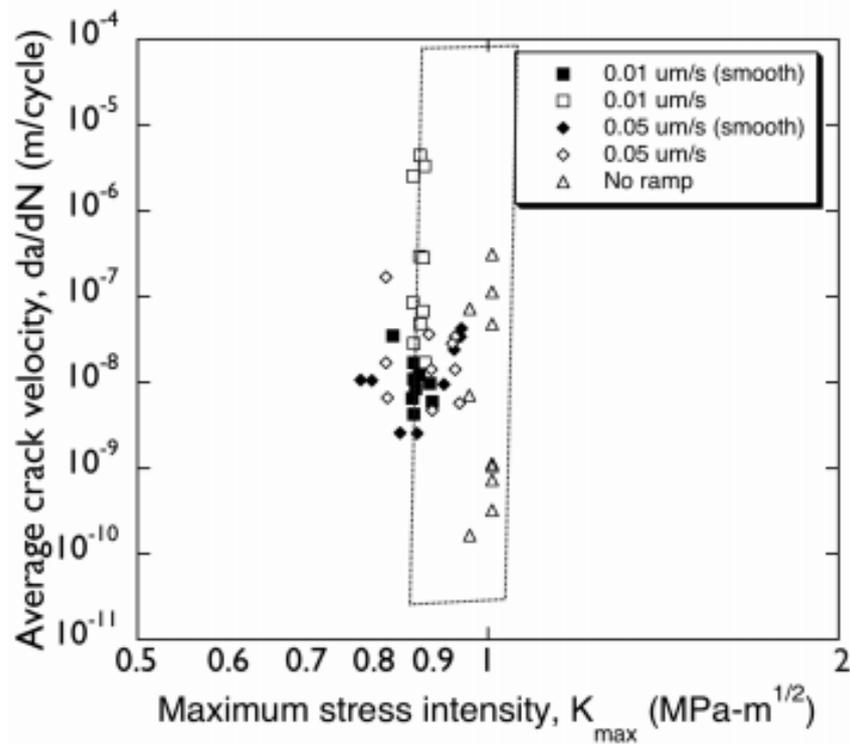


Figure 2.17: Fatigue-crack growth data, da/dN vs. K_{max} , in 150 μm thick single-crystal silicon (from different load ramps) are compared for cyclic and static fatigue tests. The area marked by the dotted line shows static fatigue test results in 50% relative humidity.[131]

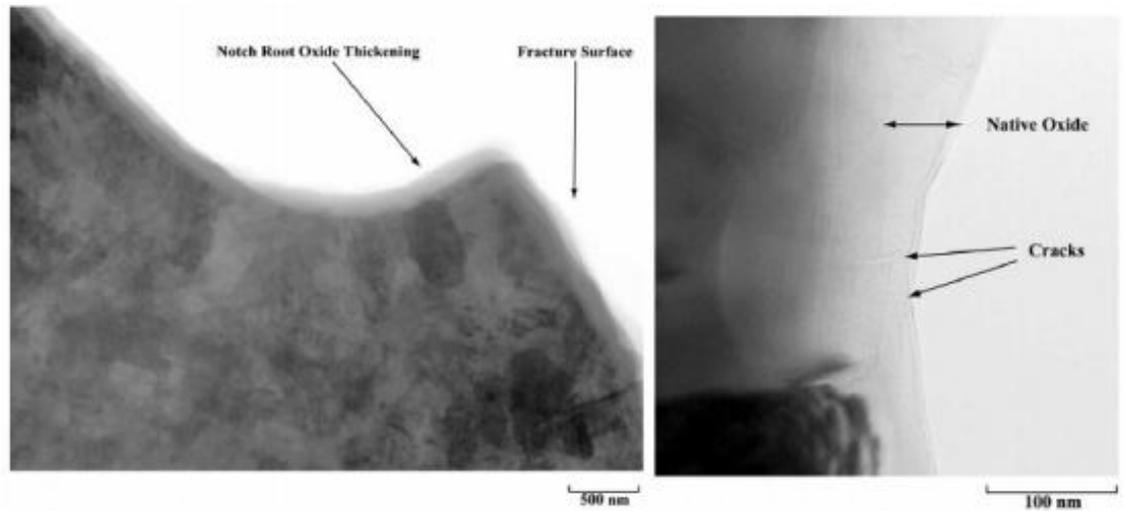


Figure 2.18: HVTEM images of the notch region in an unthinned, 2 μm thick polycrystalline silicon test sample after high-cycle fatigue. [19]

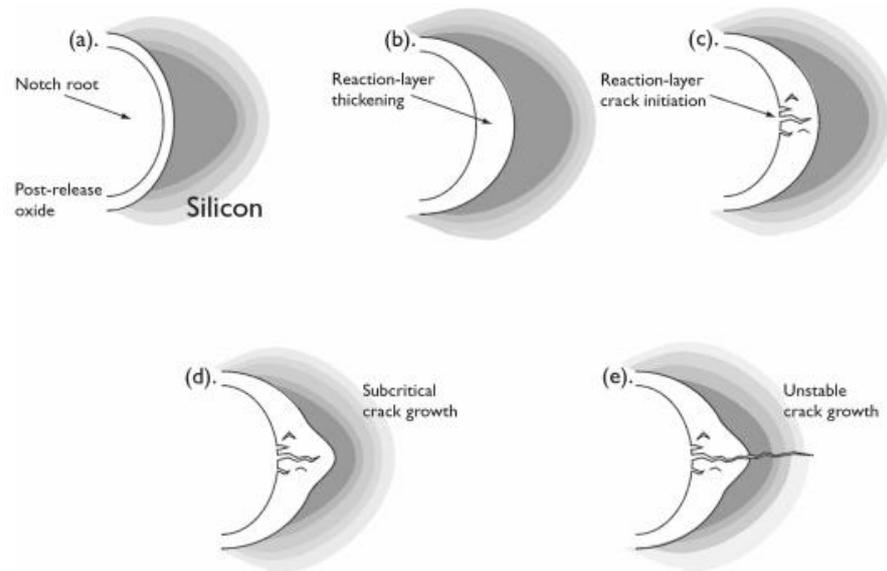


Figure 2.19: Schematic illustration of the reaction-layer fatigue mechanism for thin film fatigue at the notch of the polycrystalline silicon cantilever beam: (a) reaction layer (post-release oxide) on surface of the silicon, (b) localized cyclic stress-assisted oxide thickening at the notch root, (c) moisture-assisted crack initiation in the surface oxide at the notch root, (d) additional thickening and cracking of reaction-layer, and (e) unstable crack growth in the silicon film.[19]

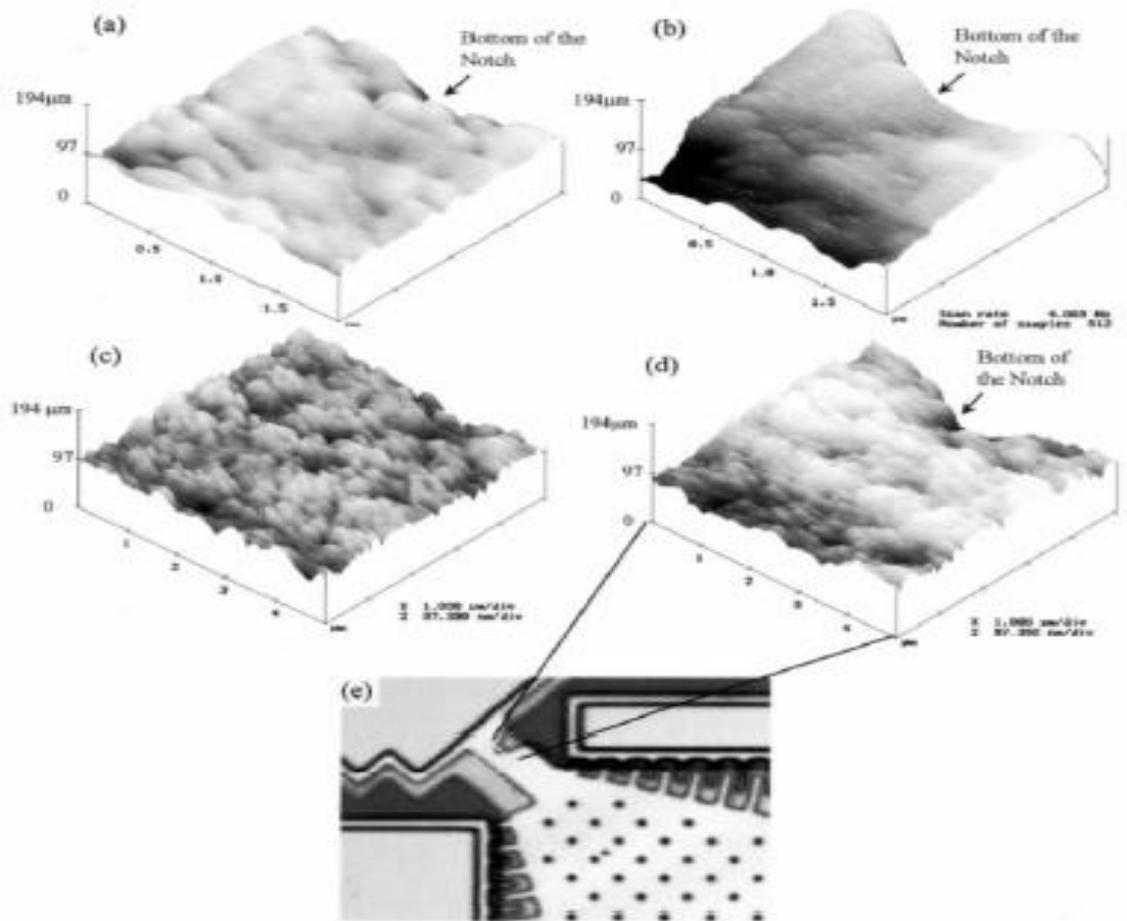


Figure 2.20: Surface topography evolution showing in a series of AFM surface scans of the area below the notch root: (a) Before actuation, (b) After the actuation of polysilicon structures for 2×10^9 cycles on a $2 \mu\text{m} \times 2 \mu\text{m}$ scale; (c) and (d) are corresponding images on a $5 \mu\text{m} \times 5 \mu\text{m}$ scale (before and after actuation, respectively), (e) Location of scan area at the vicinity of the notch root of the fatigue resonator (similar design as shown in Figure 2.15) corresponding to (a)–(d).[145].

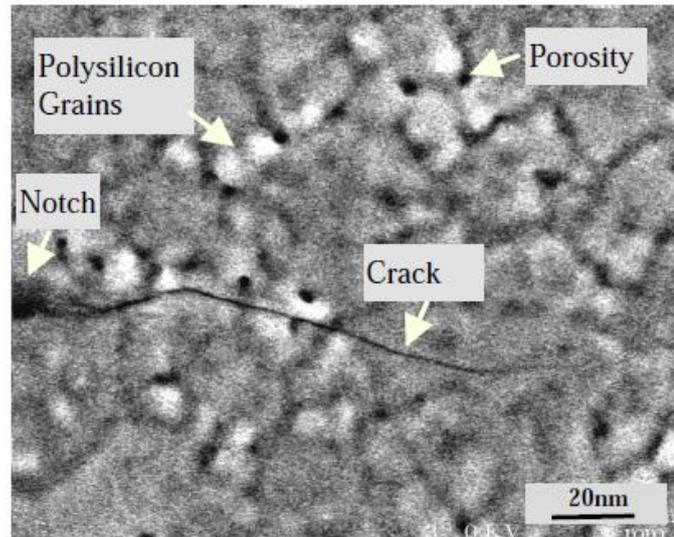


Figure 2.21: Observed Cracks in Notch Regime during fatigue crack growth. Taken from Ref

[144]

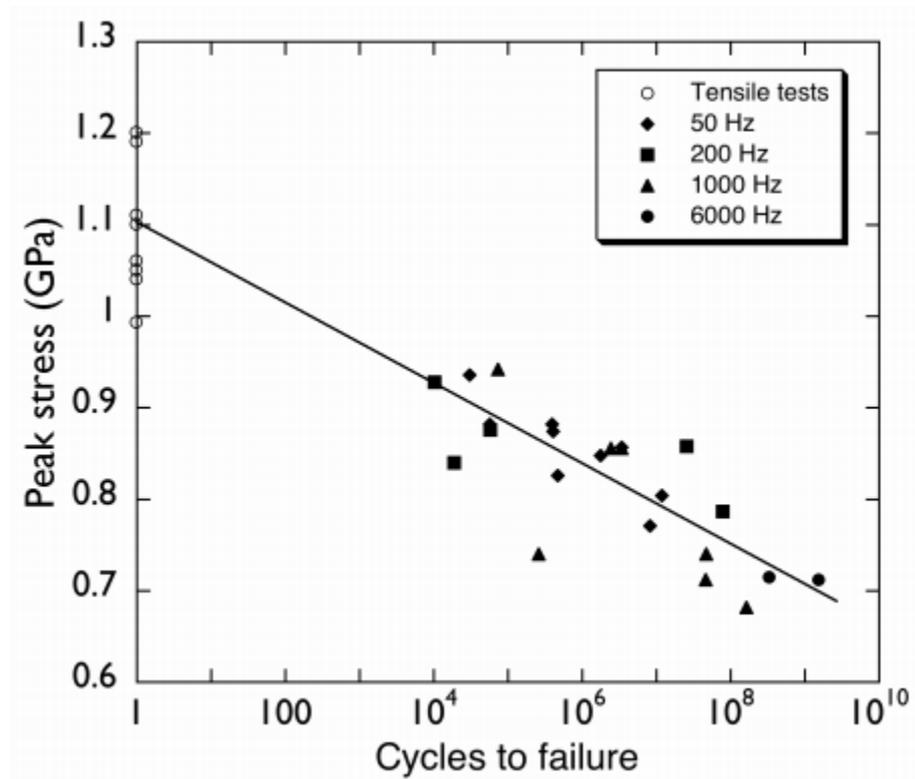


Figure 2.22: Stress-lifetime (S/N) curve of thin-film polysilicon tensile specimens during cyclic loading tested with different loading frequencies between 50 and 6,000 Hz. [168]

CHAPTER THREE

OPTICAL REFLECTANCE OF ALKALI-TEXTURED SILICON WAFERS WITH PYRAMIDAL FACETS: 2D ANALYTICAL MODEL

3.1. Introduction

Surface texturing in solar-based devices is a geometric method of reducing reflection in crystalline silicon substrates [1]. It is often achieved by the anisotropic etching of (100)-oriented silicon substrates into square-based pyramidal structures [2]. The pyramidal structures are formed by the alkaline etching of (100)-oriented silicon surfaces along crystallographic orientations that expose the {111} planes [3]. Potassium hydroxide (KOH) and additive isopropyl alcohol (IPA) are two of the most common alkaline solutions that are used for anisotropic etching of silicon surfaces [4-12]. The sizes and uniformities of the resulting pyramids are also traceable to isopropyl alcohol (IPA), which acts as a wetting agent, when added to alkaline etchants [11].

Furthermore, the pyramidal sizes, heights and base widths are usually on the order of several microns [12, 13]. Hence, the reflection falls within a basic structure that supports geometric optics [14]. Consequently, the surface texturing of (100)-oriented silicon substrates can be used to improve the absorption of light within the silicon substrates [15]. This can be achieved by using the reflection from micro-pyramids to redirect light to produce multiple reflections that increase the possibility of light absorption by silicon substrates. Since such increased absorption can enhance photo-charge conversion and solar cell efficiency, there is a need to study the effects of micro-pyramidal geometries on the reflectance of textured silicon surfaces.

In a recent work, Baker-Finch and McIntosh [16, 17] considered the reflection of normally incident light from textured silicon surfaces. They presented the reflection path and

the fraction of rays that follow a given path, using geometrical approach for regular inverted pyramidal textures and a ray tracing method for random pyramidal textures [16]. They were able to establish that, for all normally incident rays that intersect a pyramidal facet, 88.9% of incident rays experience a secondary reflection, while the remaining 11.1% experience tertiary reflection [17].

However, in practice, incident rays of sunlight are not always normal to the surfaces of textured silicon solar cells. Since the angles of incidence may vary, depending on the position on the earth, and the earth's rotation about the sun and about its own axis, there is a need to explore the possible effects of different angles of incidence on the reflection of sunlight from {111} facets on the surfaces of textured silicon solar cells. Hence, the work of Baker-Finch [16, 17] is limited to normal incidence, which is not always the case for most solar cells in service.

In this chapter, an analytical model is used to determine how incident light interacts with textured micro-pyramidal facets on alkali-textured silicon surfaces. The dependence of the secondary reflection on the angles of incidence of light rays is explored, along with the contributions of the primary and secondary reflection to the total reflection. The possible optical interactions are considered for a range of pyramidal geometries and light incidence angles. The analytical model is then used to determine the reflectances of well controlled textured surfaces. The potential for light trapping is also explored, before discussing the implications of the results for the design of micro-textured silicon surfaces.

3.2 Modeling

3.2.1 Pyramids on Etched Silicon Surfaces

The silicon solar industry relies largely on silicon wafers with (100), (110) and (111) orientations [18]. However, (100) wafers are the most geometrically appealing, since the orientations of {111} planes can be easily located on them [18]. In order to understand the

etching behavior of different wafers, it is important to know the relative positions of different crystal planes in these wafers. It is also important to know the angles that they make with each other, after etching.

During wet anisotropic etching, grooves with {111} sidewalls are exposed [14]. These are aligned with {100} planes at specific angles [15]. Also, KOH solution is the preferred etchant that is used in the anisotropic etching of silicon to produce grooves with {111} sidewalls. This is attributed to its high anisotropy against {111} planes [19, 20]. Furthermore, the angles between the individual crystallographic planes can be calculated using vector operations (dot products), since the angle between {100} and {111} planes are the same as the angles between the unit vectors of their normals. Thus, by inspection, the unit normals of both the (100) plane and the (111) plane can be obtained from their Miller indices, as shown in Figure 3.1.

In an effort to demonstrate the geometrical properties of silicon crystal on a (100) plane, the dot product (Equation 3.1) is used to obtain the angle between the (111) plane indices and the (100) plane indices to be 54.74°.

$$\hat{n}_{100} \cdot \hat{n}_{111} = |\hat{n}_{100}| |\hat{n}_{111}| \cos \theta. \quad (3.1)$$

where $|\hat{n}_{100}|$ and $|\hat{n}_{111}|$ represent the magnitudes of the unit normal vectors and θ is the angle between the (111) facet and the (100) substrate.

The above angle corresponds to that specified from Wulff's stereographic projections of a (100)-oriented silicon crystal [21]. Due to symmetry of the (111) plane on the (100) plane, the (111) plane meets the (010) plane and the (001) plane at an angle of 54.74°. The intersection of the (111) plane also forms a square-based pyramid. This implies that, for all incident light rays normal to the substrate, the primary reflections are oriented at 54.74° to the substrate surfaces. However, for actual industrial c-Si solar cells, where non-ideal etching is observed, a slightly smaller base angle (or facet tilt angle) is normally observed [16, 22].

This has been shown to be less than 52° in Refs [16, 22].

3.2.2 Textured Surface Model

3.2.2.1 Vector geometry approach

For a collimated beam of light that interacts with a textured silicon surface at a particular angle [15], the vector geometry approach explored in this section considers the possible angles of incidence of light relative to the pyramidal {111} facets. Within this context, the vector geometry approach uses vector dot products, and Phong's projection model [23], to determine the angles of the reflected rays.

Since the KOH texturing of (100) wafers forms pyramidal {111} planes [24, 25], we begin by representing the pyramidal surfaces by the vector coordinates of their plane normals. As shown in Figure 3.2, the diagonals of the pyramids are represented, respectively, by unit vectors i and j , while k is the normal to the substrate. This allows us to specify the normal vector, n , for each of the facets on the pyramid (see Figure 3.2).

Furthermore, the incident light ray is also defined by a vector, $v = -i + j - xk$ (where x is a variable). Since the normal to the substrate plane is the (001) direction, we define it as $n = k$. Thus, the dot product is used to determine the angle between v and n . This gives:

$$v \cdot n = |v||n| \cos \theta \quad (3.2)$$

where $|v|$ and $|n|$ represent the magnitudes of the vectors v and n , respectively, and θ is the angle between v and n . Hence, rearranging Equation (3.2) gives:

$$\cos \theta = \frac{-x}{\sqrt{2+x^2}} \quad (3.3)$$

With the light ray vector, v , known for a given angle of incidence (Equation 3.3), the angles of incidence of the primary reflection can be determined. Note that Equation 3.3 applies except when the incident angle is equal to 0° . When $\theta = 0^\circ$, the light ray vector is defined by $v = -k$.

Once the incident light ray vector is known, the angles of the facets can be determined from Equation 3.3. This makes it easier to obtain the secondary reflections. The coordinates of the reflected vector can be determined from the Phong model [23]. Hence, the angle of incidence of the light reflected from a surface is equal to the angle of reflection, as shown in Figure 3.3. If v is the direction of the incidence light ray vector, r is the direction of the reflected ray, n is the surface normal of the substrate, and θ_V and θ_R are the incidence and reflected angles, respectively, the reflected ray vector, r , can be determined from vector projection to be:

$$p = v \frac{|n|}{n}. \quad (3.4)$$

From Figure 3.3, p is a projection of v onto n . Thus, we may rearrange Equation 3.4 to obtain:

$$\cos \theta = \frac{|p|}{|v|}. \quad (3.5)$$

Also, using the dot product of two vectors, we may express $\cos \theta$ as:

$$\cos \theta = \frac{v \cdot n}{|v| |n|}. \quad (3.6)$$

By combining Equations (3.4), (3.5) and (3.6), p becomes

$$p = \frac{v \cdot n}{|v| |n|} n. \quad (3.7)$$

Since vector q connects v to its projection and also connects p to r (see Figure 3.3), the coordinates of the reflected vector r is given by:

$$r = 2 \frac{v \cdot n}{|v| |n|} n - v. \quad (3.8)$$

As an example, consider the case of light under normal incidence to the substrate, Equation 8 can be used to calculate the secondary reflection for a given light ray ($v = -k$) that is incident to a facet with $n_1 = i + j + k$. The secondary reflection occurs on a neighbouring facet with $n_2 = -i - j + k$. Thus, by combining Equations 3.6 and 3.8, $\theta = \cos^{-1} (5/\sqrt{27})$, which is equal to 15.79° . This implies that, for normal incidence to a textured silicon (100) substrate, all secondary reflections occur at an angle of 15.79° .

The above method represents on possible approach to the determination of the angles between any incoming ray of light and any pyramidal facet. However, it does not treat cases in which fractions of the light rays are incident on different facets. Furthermore, the method does not determine whether reflection actually occurs or not. These issues can be addressed by exploring simpler systems, such as periodic two-dimensional (2D) arrangements of textured pyramids that will be considered in the next section.

3.2.2.2 2D Model of Periodic Pyramidal Structures

(A) Basic Assumptions

A 2D model of a periodic pyramidal system is illustrated schematically in Figure 3.4. This can be achieved in practice by masking the surface of a silicon wafer prior to the etching process [20]. Assuming that the incident light rays are perpendicular to the surface of the substrate, the optical interaction of light (with the separate facets X and Y) can be idealized, as a two-dimensional problem.

In an effort to determine whether the angle of incidence, prior to the primary reflection on surface X, can produce secondary reflections, we gradually increase the angle of incidence from $\theta = 0^\circ$ to $\theta = 35.3^\circ$ until the incident light ray is tangential to facet Y (Figure 3.4). Above 35.3° the reflections from facet Y vanish until $\theta = 54.7^\circ$, at which the incident ray becomes normal to facet X. Furthermore, for incident angles greater than 54.7° , the reflected rays are directed away from the substrate and not towards it. Hence, secondary reflection will not occur for angles of incidence greater than 54.7° .

(B) Contributing Factors from Primary, Secondary and Total Reflectances

To estimate the total reflectance, the fraction of light rays that is incident to each facet is estimated along with their contributions to the total reflectance. As shown in Figure 3.4, angles θ_x and θ_y are the angles between the light ray and the normal vectors to facets X and Y,

for primary reflections. Hence, the fraction of the light ray that falls on each facet can be expressed simply as the ratio of that angle's cosine to the sum of both angles' cosines. This is given by:

$$F_{X1} = \frac{\cos(\theta_X)}{\cos(\theta_X) + \cos(\theta_Y)} \quad F_{Y1} = \frac{\cos(\theta_Y)}{\cos(\theta_X) + \cos(\theta_Y)} \quad (3.9)$$

F_{X1} and F_{Y1} are the contributing factors of the primary reflections from facets X and Y, respectively. Since all of the reflections from facet Y vanish for angles greater than 35.3° , Equation 3.9 is only valid for angles, θ , up to 35.3° . Beyond $\theta = 35.3^\circ$, $F_{X1} = 1$ and $F_{Y1} = 0$. For secondary reflections from facet Y, the fractional contributing factor, $F_{Y2} = 1$, since any light ray reflected from facet Y experiences a secondary reflection.

Unlike factor F_{Y2} , the contributing factor (F_{X2}) of the secondary reflections from facet X is more complex. By inspection, the contributing factor F_{X2} varies from 1 to 0, for four separate cases in the angle of incidence. In the first case, when the angle of incidence (to the substrate) is less than 19.4° , secondary reflection occurs on the neighbouring Y facet, for all light rays that strike any arbitrary point on facet X. Secondly, for angles of incidence between 19.4° and 35.3° , some of the light rays reflected from facet X are directed away from the substrate, while those at angles of incidence between 35.3° and 54.7° are not able to strike some portion of facet X, due to shading from facet Y. Finally, at any angle greater than 54.7° , secondary reflections can no longer occur.

For any angle of incidence between 19.4° and 35.3° , as illustrated in Figure 3.5, secondary reflection does not occur between points M and B on facet X (i.e. line length MB). Therefore, the fraction of facet X that does not produce secondary reflections from incident light rays is simply the ratio of the MB to MO. From Figure 3.5, the base length of the pyramid is equal to the distance between the peaks of the two pyramids. This implies that MH

is twice the line length, a , shown in Figure 3.5. Hence, the line length, a , can be related to the side length, L , via the following expression:

$$a = L \cos \theta \quad (3.10)$$

Hence, for $\theta = 54.7^\circ$, Equation 3.10 gives $a = L \cos (54.7) = L/\sqrt{3}$.

Since MH is twice the length of the line segment, a , MH is now given by:

$$MH = 2a = 2L/\sqrt{3}.$$

Furthermore, applying the sine rule to triangle HMB, we obtain:

$$\frac{\sin(\alpha)}{MB} = \frac{\sin(125.3 - \alpha)}{MH} \quad (3.11)$$

Substituting $MH = 2L/\sqrt{3}$ into Equation 3.11 now gives:

$$\frac{\sin(\alpha)}{MB} = \frac{\sin(125.3 - \alpha)}{\frac{2L}{\sqrt{3}}} \quad (3.12)$$

Hence, rearranging Equation 3.12 now gives:

$$\frac{MB}{L} = \frac{\frac{2}{\sqrt{3}}\sin(\alpha)}{\sin(125.3 - \alpha)} \quad (3.13)$$

Thus, the relationship between the angle of incidence, θ , and the angle, α , opposite to the line length MB, can be obtained by applying the sine rule to triangle MHB. Since the incidence light ray is reflected across the normal to the line MB, we can also equate the included angle to 90° . That gives:

$$\gamma + \theta + 35.3^\circ = 90^\circ \quad (3.14)$$

Rearranging Equation 3.14 now gives

$$\gamma = 54.7^\circ - \theta$$

Also, from triangle MCB, we can deduce that:

$$2\gamma + \theta = 90^\circ - \alpha \quad (3.15)$$

Hence, $2(54.7^\circ - \theta) + \theta = 90^\circ - \alpha$, and α is now given by

$$\alpha = \theta - 19.4^\circ \quad (3.16)$$

Hence, substituting Equation 3.15 into Equation 3.13 now gives:

$$\frac{MB}{L} = \frac{\frac{2}{\sqrt{3}}\sin(\theta-19.4^\circ)}{\sin(144.7^\circ - \theta)} \quad (3.17)$$

Thus, the contributing factor, F_{X2} , of the secondary reflections for this range is given by:

$$F_{X2} = 1 - \frac{MB}{L} = 1 - \frac{\frac{2}{\sqrt{3}}\sin(\theta-19.4^\circ)}{\sin(144.7^\circ - \theta)} \quad (3.18)$$

For angles of incidence between 35.3° and 54.7° (Figure 3.6), part of facet X between points O and A (line length OA) does not have access to light rays due to the effects of shading. The proportion of facet X that is not accessible to light rays can thus be expressed as the ratio of the OA to the side length of the pyramid, OM or L.

Hence, by applying the sine rule to triangle HOA, we obtain:

$$\frac{\sin(\beta)}{OA} = \frac{\sin(109.4 - \beta)}{L} \quad (3.19a)$$

Rearranging Equation 3.19 now gives:

$$\frac{OA}{L} = \frac{\sin(\beta)}{\sin(109.4 - \beta)} \quad (3.19b)$$

Furthermore, by substituting the angle, β , with the expression $\beta = \theta - 35.3^\circ$, we have:

$$\frac{OA}{L} = \frac{\sin(\theta-35.3^\circ)}{\sin(144.7-\theta)} \quad (3.20)$$

Thus, the contributing factor, F_{X2} , of the secondary reflections for this range is given by:

$$F_{X2} = 1 - \frac{MB}{L} - \frac{OA}{L} = 1 - \frac{\frac{2}{\sqrt{3}}\sin(\theta^\circ - 19.4^\circ)}{\sin(144.7^\circ - \theta^\circ)} - \frac{\sin(\theta - 35.3^\circ)}{\sin(144.7 - \theta)} \quad (3.21)$$

So for all angles, F_{X2} can be obtained via any of the following expressions, depending on the range of the angle of incidence of the light rays:

$$F_{X2} = \begin{cases} 1 & \theta \leq 19.4^\circ & (3.22a) \\ 1 - \frac{\frac{2}{\sqrt{3}}\sin(\theta^\circ - 19.4^\circ)}{\sin(144.7^\circ - \theta^\circ)} & 19.4^\circ \leq \theta \leq 35.3^\circ & (3.22b) \\ 1 - \frac{\frac{2}{\sqrt{3}}\sin(\theta^\circ - 19.4^\circ) + \sin \theta^\circ - 35.3^\circ}{\sin(144.7^\circ - \theta^\circ)} & 35.3^\circ \leq \theta \leq 54.7^\circ & (3.22c) \\ 0 & \theta \geq 54.7^\circ & (3.22d) \end{cases}$$

By combining the primary and secondary reflections with their contributing factors, the total reflectance can be obtained from the following expression [26, 27]:

$$R_T = R_{X1}F_{X1}[R_{X2}F_{X2} + (1 - F_{X2})] + R_{Y1}F_{Y1}R_{Y2} \quad (3.23)$$

where R_{X1} and R_{Y1} are the primary reflection coefficients from facets X and Y, with contribution factors of F_{X1} and F_{Y1} , respectively. R_{Y2} is the secondary reflection coefficient from facet Y. The secondary reflection coefficient from facet X is represented by R_{X2} with its contribution factor being F_{X2} . However, $(1 - F_{X2})$ accounts for the light not subjected to a secondary reflection from facet X. The reflectance, R , for both the primary and secondary reflections can be obtained using the Fresnel equations adopted from Ref. [28]. These give:

$$R = |r|^2 = \left(\frac{\cos(\theta) - \sqrt{\left(\frac{n_{Si}}{n_{air}}\right)^2 - \sin^2(\theta)}}{\cos(\theta) + \sqrt{\left(\frac{n_{Si}}{n_{air}}\right)^2 - \sin^2(\theta)}} \right)^2 \quad (3.24)$$

where r represents the reflection coefficient for both the primary and secondary reflections.

3.3 Experimental Procedures

In an effort to validate the pyramidal structures used in the above model, (100)-oriented silicon wafers were procured from Semiconductor Wafer Inc., Hsinchu, Taiwan. Prior to alkaline etching, the wafers were dipped in 0.5% HF for 100s to remove native oxides and subsequently dried in nitrogen gas. Samples were etched in alkaline solution of KOH under the etching conditions of etch duration of 40 minutes, etch temperature of 80°C and a volume concentration of KOH: IPA in the ratio 2:4. Also, at the end of each texturing process, the samples were rinsed in distilled de-ionized water and dried in nitrogen gas.

The alkaline etching was carried out in a GFL-1083 thermo-coupled water bath (Gesellschaft für Labortechnik (GFL), Burgwedel, Hanover, Germany). Scanning electron images of the etched and unetched silicon surfaces were then obtained using an EVO MA-10 Scanning Electron Microscope that was operated at 10kV (EVO MA-10, Carl Zeiss, Hamburg, Germany).

3.4. Results and Discussion

3.4.1 Reflection from Etched 100 Silicon Surfaces

A secondary electron image of an etched 100 oriented silicon wafer surface is presented in Figure 3.1. This shows clearly that pyramidal facets are formed on the silicon wafer, after etching. This has geometrical characteristics that are similar to those discussed and idealized earlier in section 3.2. However, unlike the idealized unit cell structures, in which the pyramidal dimensions were uniform, the actual pyramidal structures exhibited variations in the unit cell heights, although the basic shapes were geometrically similar. The interactions with the incident light rays should, therefore, apply to primary reflections, since the secondary reflections may be affected by differences in the adjacent facets.

As discussed in the preceding section, the possibility that the incident light will experience a secondary reflection (double-bounce incidence) or a multiple reflection, depends upon the height of the pyramid, the apex angle of the pyramid and the facet tilt angles of the geometrical textures, with respect to the surface of the wafer [29, 30]. From prior work by Sethi *et al.* [31], a secondary reflection is experienced or guaranteed, if the facets tilt angle falls within the range between 45° and 60° . Since texturing of (100)-oriented silicon wafers in alkaline solution produces pyramids with apex angles of 70.6° and facet tilt angles of 54.7° for an ideal process or $<52^\circ$ for non-ideal process [16, 22], which are within the range specified by Sethi *et al.* [31], our model can be used to investigate the possibility of secondary reflection, for the full range of incidence angles to the substrate.

By inspection, when the angle of incidence to the substrate is less than 19.4° , secondary reflection occurs on the neighbouring Y facet, for all light rays that strike any arbitrary point on X facet. This validates prior work on the reflection of normally incident light rays using the OPAL 2 software [32, 33] to show that 88.9% of incident rays experience a double and 11.1% experience triple bounce. However, if the angle of incidence is between 19.4° and 35.3° , some light is reflected from facet X. The reflected light is directed away from the substrate, leaving only some proportion of the facet to experience secondary reflection.

In the case of incident angles between 35.3° and 54.7° , the incident light rays are not able to strike some portion of facet X. This is due to shading from facet Y. However, for incident angles equal to 54.7° , the possibility of secondary reflections is eliminated because the incident light is perpendicular to facet X. Thus, at any angle greater than 54.7° , secondary reflections cannot occur. Hence, any incident light rays that strike the textured surfaces of etched (001)-oriented silicon surfaces at low incidence angles produces more secondary reflections and thus have at least two chances of being absorbed. However, the chances of

absorption are reduced at high incidence angles, where most of the reflected light rays are directed away from the substrate.

3.4.2 Total Reflectance

It is important to note here that the above model does not account for the tertiary reflections, as with prior work on the reflection of normally incident sunlight [16, 17, 22]. These were not explored, since they do not occur often for non-normal incident angles [31]. Furthermore, they have only a minor effect on the overall accuracy of the total reflectance.³¹ Also, in the 2D textured surface model, the pyramids were assumed to be aligned with one another, as shown in Figure 3.4. However, this is valid only for regular inverted pyramidal textures and not for randomly textured silicon wafers. Hence, a more realistic approach is needed to model the light/pyramid interactions in actual etched (001)-oriented silicon wafers with textures similar to those presented in Figure 3.1. Nevertheless, the results obtained from the current idealized 2D textured surface model are close to the measured reflectance values presented by Parretta *et al.* [20].

A summary of the contribution factors (F_{X2}) obtained for different angles of incidence is presented in Figure 3.7. This shows that, above the incident angle of 19.4° , F_{X2} decreases gradually with increasing angle of incidence. Furthermore, the dependence of the total reflectance on the angle of incidence is presented in Figures 3.8a and 3.8b, for etched (001)-oriented surfaces subjected to incident light rays with a wavelength, λ , of 635 nm. In all cases, the total reflectances of the textured surfaces are lower than those of the flat polished surfaces.

The predicted values of reflectance (obtained from Equation 3.23) are also in good agreement with the measured reflectance values (Figure 3.8c). The close agreement between the experimental and predicted reflectances suggests that the idealized model presented here captures most of the important aspects of light interactions with the pyramidal structures that

are formed by the alkaline etching of (001)-oriented silicon surfaces with etchants such as KOH.

3.4.3 Implications

The implications of the above model are quite significant. First, they show that more secondary reflections are experienced on textured silicon (100)-oriented wafers at low incidence angles. The optical path lengths also increase with increasing secondary reflections, thus, providing increased chances of light absorption. This suggests that KOH textured pyramidal structures can be tailored to control their reflectance, when the angle of incidence of light and the uniformity of the pyramids are well controlled.

Furthermore, the good agreement between the measured and the predicted reflectances suggests that our 2D model captures most of the important aspects of light interactions with the pyramidal structures that are formed by the KOH-etching of (001)-oriented silicon surfaces.

These resulting reductions in surface reflectance enable more light to be trapped for conversion to charge in single crystal silicon solar cells. The control of alkaline etching can, therefore, be used to engineer the improvement of silicon solar cell efficiency. Further work is clearly needed to explore the possible improvements in solar cell efficiency that can be achieved via the controlled alkaline etching of silicon wafers in silicon solar cells.

3.5. Conclusions

1. In this chapter, a simple analytical model has been developed and used to study the optical behaviour of flat and textured silicon substrates. The model explored the possibility of secondary reflections, for the full range of incidence angles to the silicon substrate. The geometrical interactions of light rays with pyramidal facets were used to predict the

reflectance values, which were compared with measurements of reflectance on alkaline textured silicon surfaces.

2. Secondary reflection is experienced or guaranteed, for all pyramid heights, when the angle of incidence to the substrate is less than 19.4° . Hence, any incident light beams that strikes the textured surfaces of etched (001)-oriented silicon surfaces at low incidence angles, produces more secondary reflections than flat silicon substrates. Thus, secondary reflections increase the time available for the incident light rays to be absorbed into (001)-oriented silicon single crystals.

3. The predictions obtained from the current 2D textured surface model are close to the measured reflectance values presented in Ref. [20]. The close agreement between the experimental and predicted reflectances suggests that the idealized model presented here captures most of the important aspects of light interactions with the pyramidal structures that are formed by the alkaline etching of (001)-oriented silicon surfaces with etchants such as KOH.

4. The current results suggest that the model can be helpful in the design of textured silicon surfaces for the control of surface reflectance and the trapping of light by secondary reflections. Such control and trapping could lead to increased photo-conversion and silicon solar cell efficiency.

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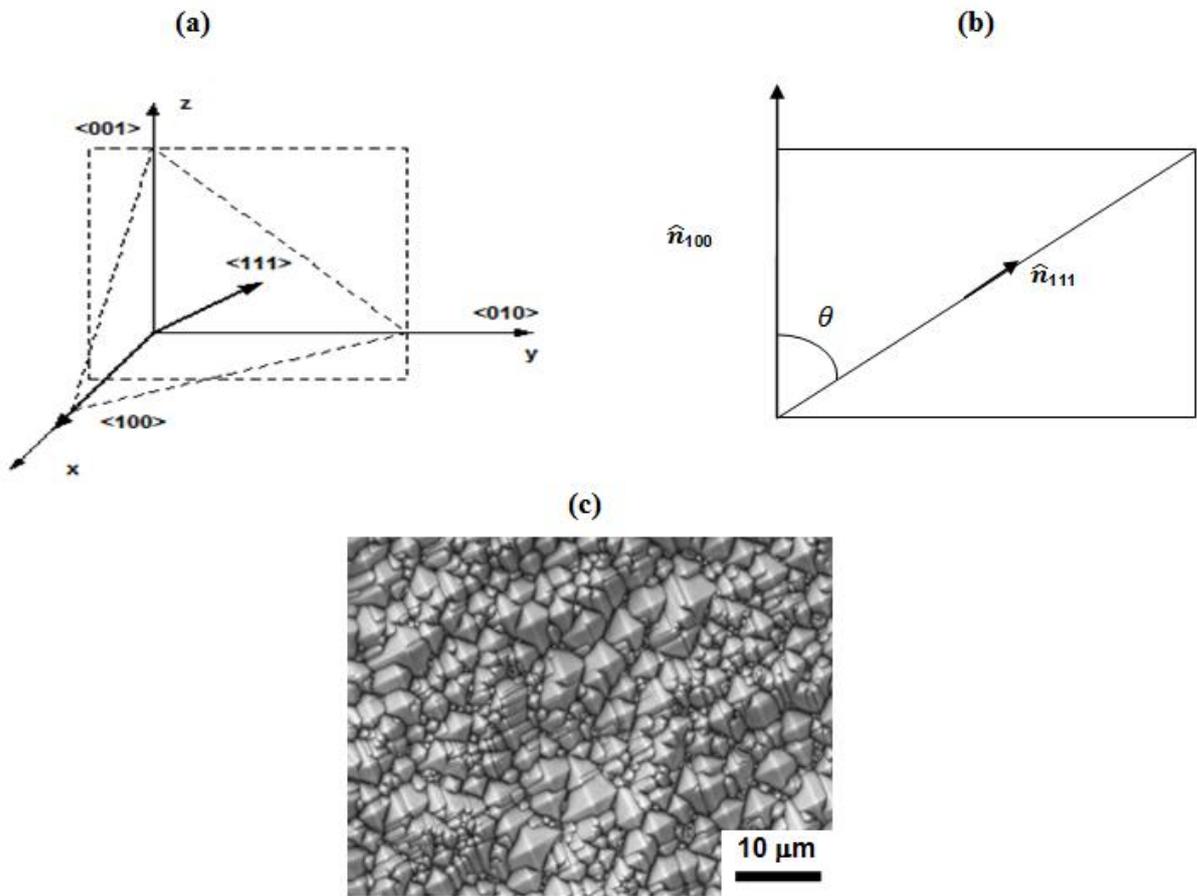


Figure 3.1: (a) the square and triangular shapes represents the (100) plane and (111) plane respectively (b) a rectangle including the main diagonal of the cube used to determine the angle of interest (c) SEM image of pyramids on the surfaces of KOH etched (001) silicon wafers.

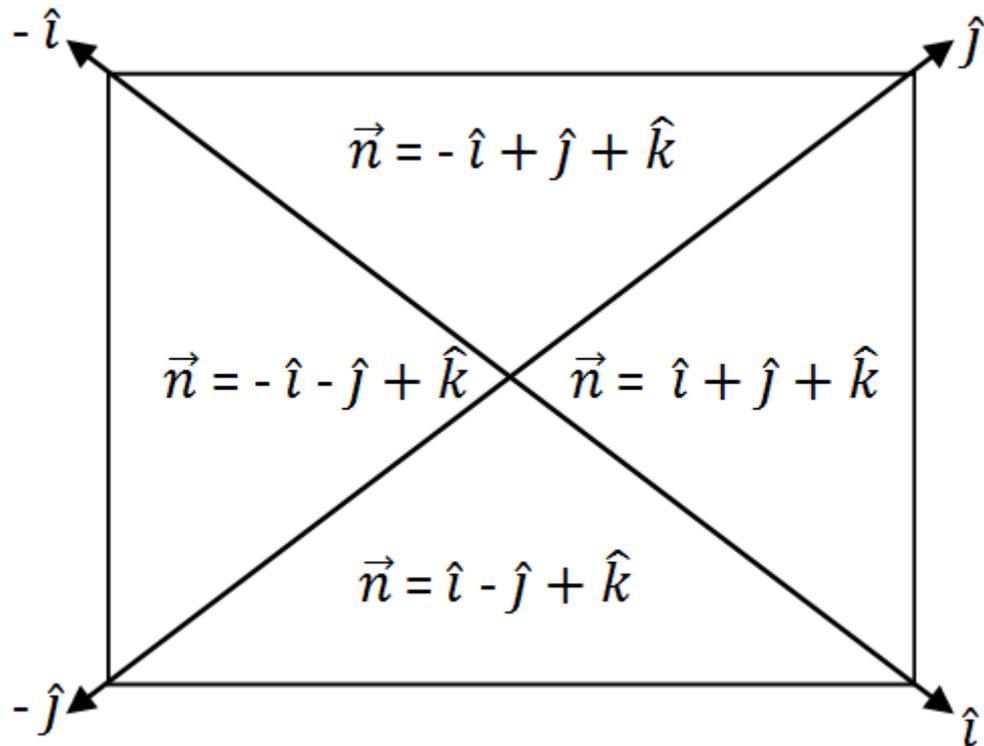


Figure 3.2: Top view of a square based pyramid showing the unit vectors and normal vectors on the textured surface.

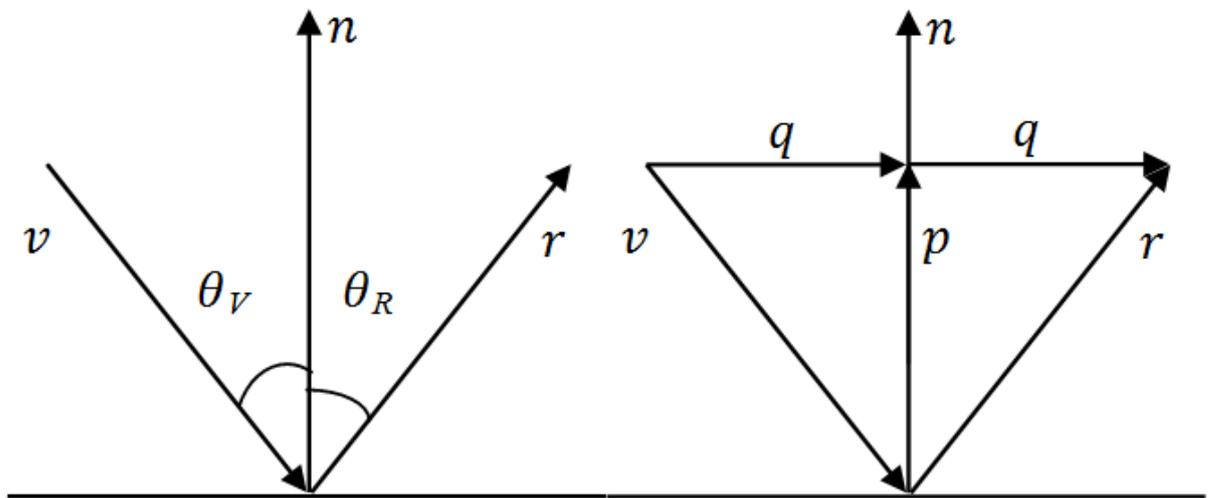


Figure 3.3: Phong reflection model showing the vector projection of the incidence light ray.

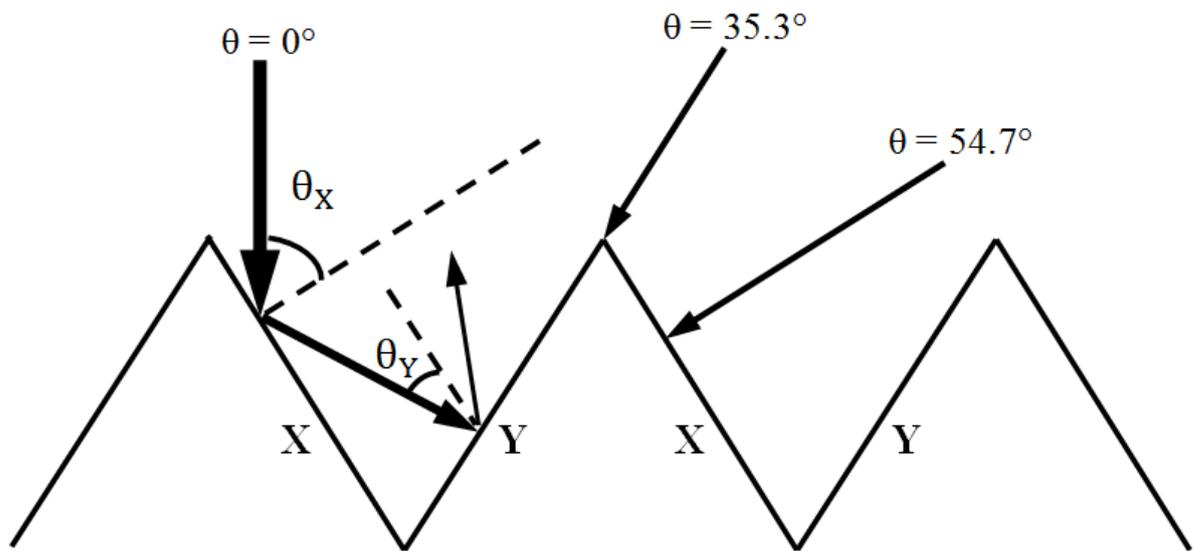


Figure 3.4: The schematic diagram of the side view of a periodic pyramidal system.

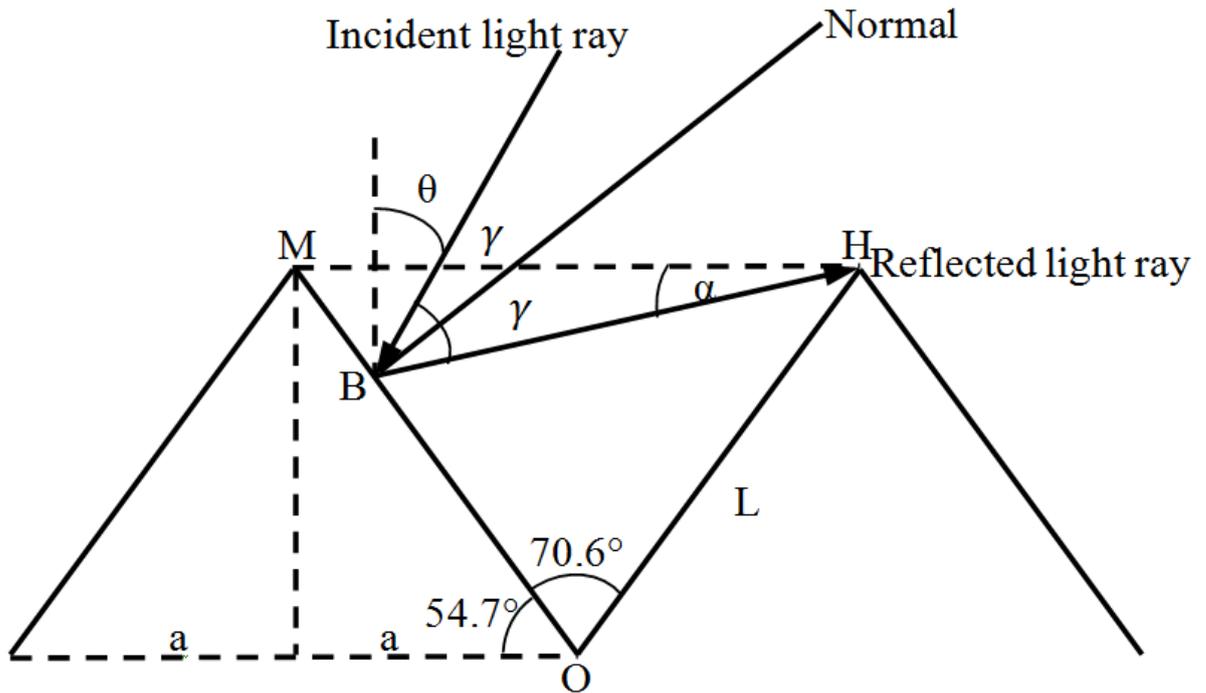


Figure 3.5: Light interaction with the pyramid facet at an angle between 19.4° and 35.3° .

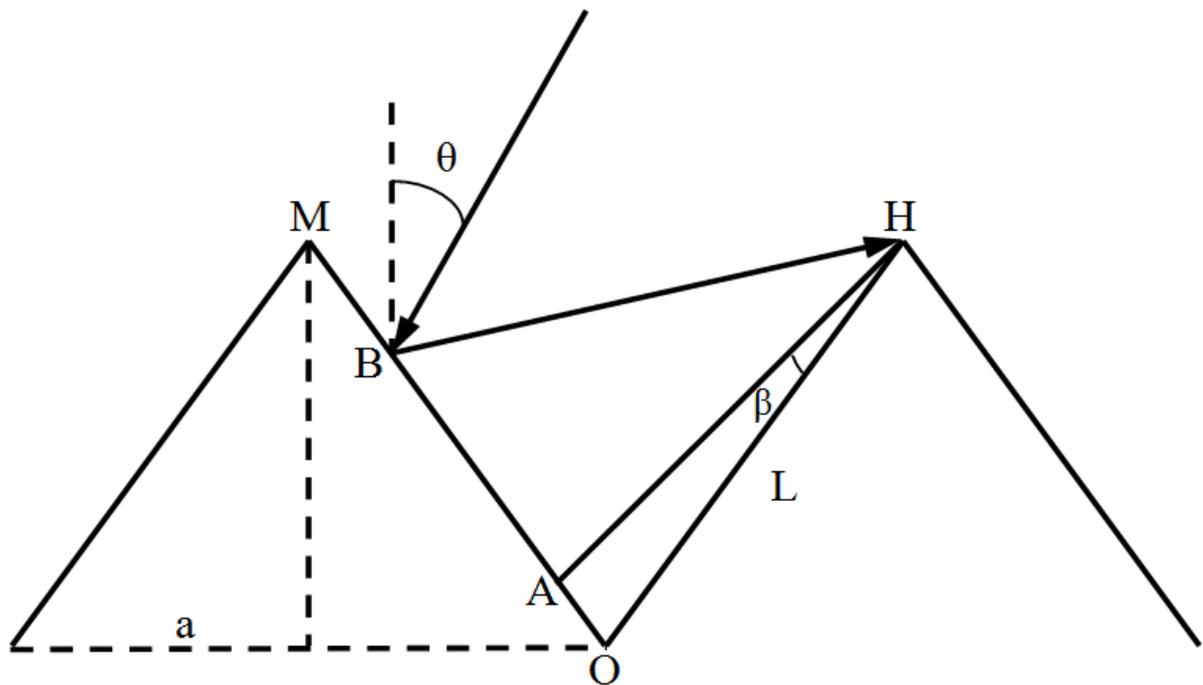


Figure 3.6: Light interaction with the pyramid facet at an angle between 35.3° and 54.7° .

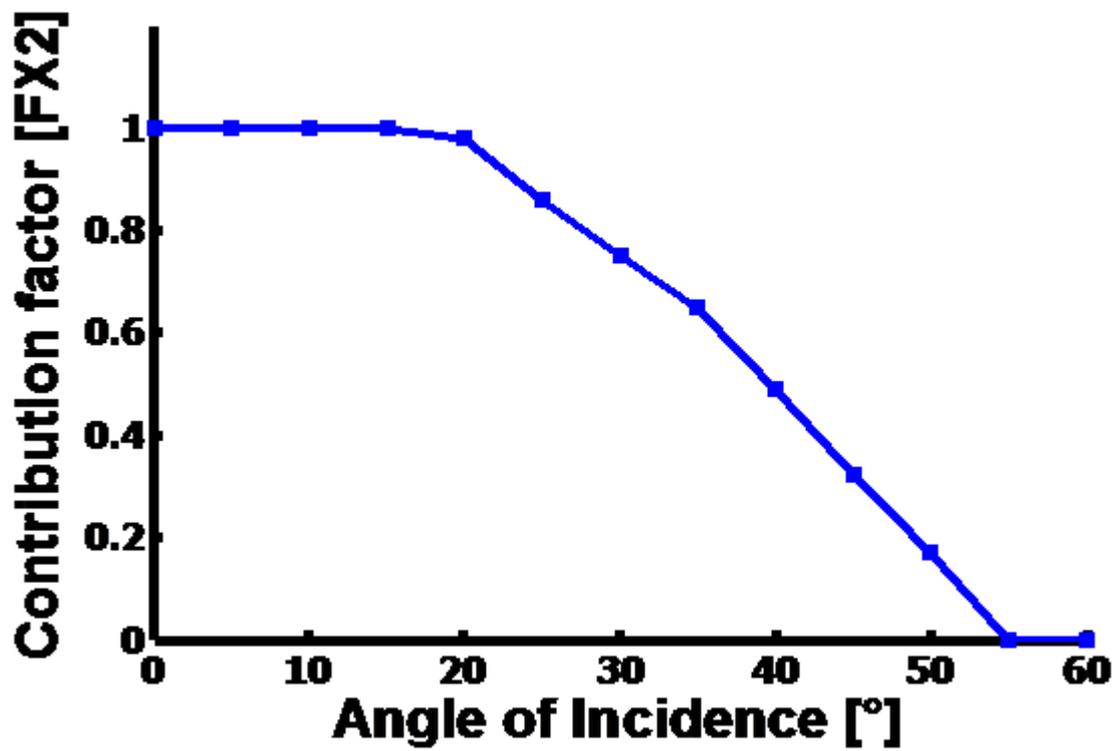


Figure 3.7: The dependence of F_{X2} on the incidence angle.

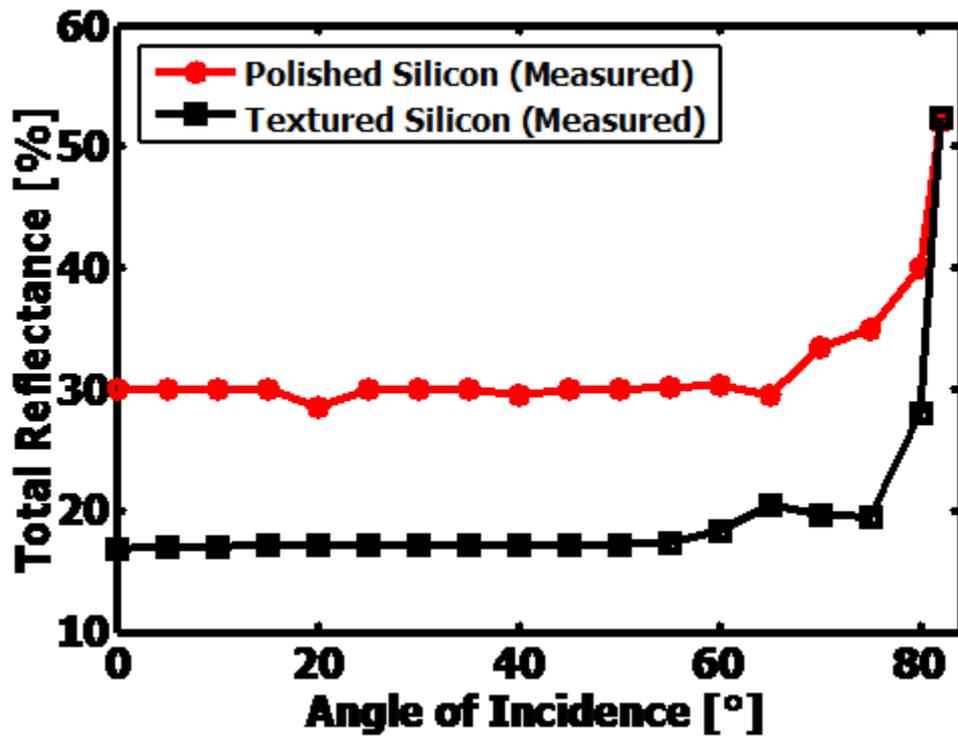


Figure 3.8a: Measured total reflectance versus angle of incidence treatments at $\lambda = 633$ [20].

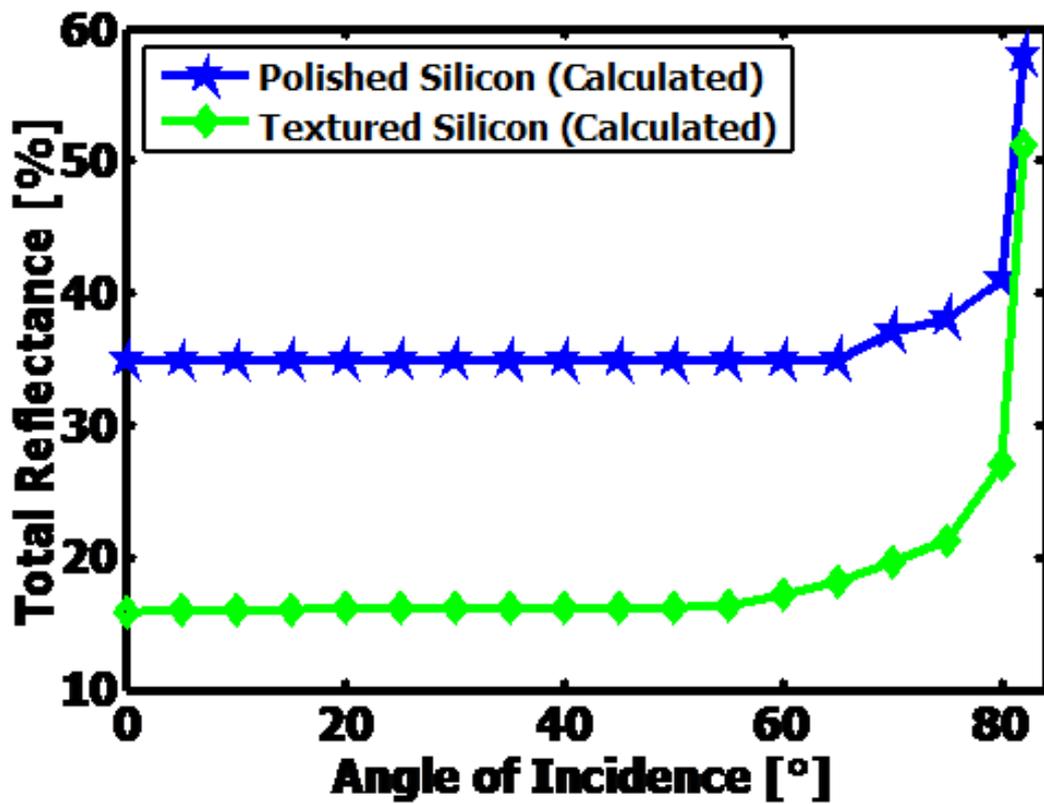


Figure 3.8b: Calculated total reflectance versus angle of incidence treated at $\lambda = 635$.

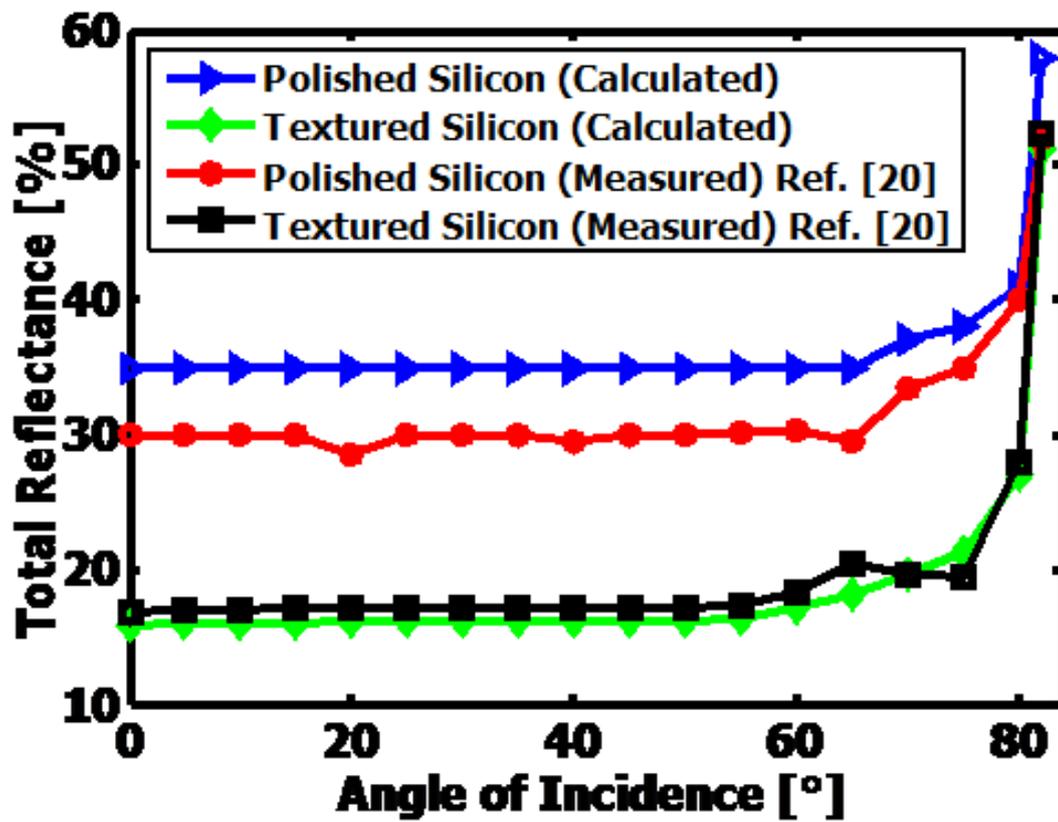


Figure 3.8c: The calculated and measured reflectance versus angle of incidence.

CHAPTER FOUR

SURFACE TEXTURE AND OPTICAL PROPERTIES OF CRYSTALLINE SILICON SUBSTRATES

4.1 Introduction

The interest in the application of solar photovoltaic (PV) cells has led to the introduction of a variety of solar panels for commercial purposes [1, 2]. These includes the solar powered traffic lights and CCTV cameras, solar water pumps, solar street lighting systems, and mini-grid solar PV panels for rural electrification. However, in such panels, particularly the silicon-based solar panel, the absorption of sunlight is relatively weak [3]. This is partly because of the optical losses that occur due to the high refractive index (approximately 3.5) of crystalline silicon at solar wavelengths [3]. This reduces the efficiencies of crystalline silicon solar cells to levels between ~12 and 20% [4].

Hence, in order to increase the efficiencies of the silicon-based cells, there is a need to reduce the optical reflectance of silicon wafers. This is especially important for wavelengths in the visible and near-IR spectrum [5]. The need has also stimulated significant research efforts in the silicon solar research community to explore a number of approaches to reduction of the optical reflectance of silicon solar cells over the past 45 years [4-8]. Within this context, surface texturing represents a promising approach that can be used to engineer surface reflection and light absorption on the surfaces of the silicon solar cells.

Surface texturing involves the control of surface morphology by etching [9], photolithography [10] or laser-based [11] techniques that can be used to control the interactions of light with silicon surfaces. Solutions of potassium hydroxide (KOH) and isopropyl alcohol (IPA) are the two most common alkaline etchants that are used for the anisotropic etching of silicon surfaces. These etchants are used due to their relatively low cost

and high capacity for anisotropic etching of silicon surfaces with improved light trapping characteristics [12-18]. However, the effect of anisotropic etching (on the morphology of silicon surfaces) also depends strongly on wafer orientation [19]. Consequently, (001) substrates are textured to form square-based pyramids for the effective trapping of light in crystalline-silicon (c-Si) solar cells [17]. Such pyramidal structures are formed as a result of interactions between the alkaline solutions and silicon surfaces along {111} planes [18].

The pyramids that are produced are with apex angles of 70.6° and facet tilt angles of 54.7° for an ideal process [20, 21] or 45° - 52° for non-ideal process [22, 23]. Furthermore, the pyramidal sizes, heights and base widths are usually on the order of several microns [24, 25]. Consequently, the surface texturing of (100)-oriented silicon substrates can be used to improve the absorption of light within the silicon substrates [8]. This can be achieved by using the reflections from micro-pyramids to redirect light to produce multiple reflections that increase the possibility of light absorption by silicon substrates (Figure 4.1b). However, for effective light absorption or multiple reflections, there must be uniformity in the sizes of the pyramids, similar to those of regular inverted pyramidal structures [26, 27].

In recent work, Xun *et al.* [28] suggested that sizes and uniformities of pyramidal structures are traceable to amount of IPA that is often added to KOH as a wetting agent, during the surface texturing process. However, the role of IPA (in the alkaline texturing process) is not fully understood [29], although prior work has explored the effects of KOH and IPA etching on the surface morphology of silicon wafers [13, 14, 28-34]. There is, therefore, a need for further studies to determine the ratios of IPA to KOH that are needed for the control of silicon surface textures to minimize the reflection of incident sunlight, while trapping the light for photoelectric conversion.

This chapter presents the results of an experimental study of the effects of KOH/IPA etching on the stability of pyramidal textures on the (001)-oriented silicon wafers. The effects

of etchant concentration and KOH/IPA ratio are explored, along with the effects of etching duration and temperature. The resulting surface morphologies are characterized with atomic force microscopy (AFM), scanning electron microscopy (SEM) and surface profilometry (SP). The optical reflectance associated with the different surface textures is also determined using Ultra-Violet (UV)-visible Spectroscopy. In order to ascertain the compatibility of texturing process with light trapping mechanism, simple $1 \times 1 \text{ cm}^2$ solar cell devices (with the structure of ITO/p-Si/Al) were fabricated on substrate with both textured and un-textured surfaces before discussing the implications of the results for the development of silicon solar cells with improved photo-conversion efficiencies.

4.2 Experimental Procedures

4.2.1 Substrate Preparation

The (001)-oriented p-type silicon wafers that were used in this study were obtained from Semiconductor Wafer, Inc., Hsinchu, Taiwan. The wafers had square dimensions of $1 \text{ cm} \times 1 \text{ cm}$, a thickness of $275 \text{ }\mu\text{m}$ and a resistivity of $1 \text{ }\Omega\text{-cm}$. Prior to texturing, the wafers were dipped in 0.5% HF for 100 s, before rinsing them in distilled deionized water and drying in nitrogen gas. The texturing process was done in a GFL-1083 thermo-coupled water bath (Gesellschaft für Labortechnik (GFL), Burgwedel, Hanover, Germany). The studies explored the effects of: (i) etchant concentration; (ii) process temperature; and (iii) process duration. For each set of experiments, one parameter was varied, while keeping the other two variables constant.

The process parameters are summarized in Table 4.1. This shows that the etching times were varied between 30 and 60 minutes, in steps of 10 minutes, while keeping the temperature and concentration constant. Similarly, the etching temperatures were varied

between 50⁰C and 90⁰C. This was done in steps of 10⁰C, while maintaining the etching time and concentration constant.

Finally, the texturing process was performed at different concentrations (g/ml) and volume ratios of KOH and IPA, respectively, while keeping the etching time and etching temperature constant. The textured samples were then rinsed in distilled deionized water and dried in dry nitrogen gas, after each texturing process.

4.2.2 Optical Characterization and Surface Morphology

The optical reflectance of the textured samples was measured using an Avantes Optics UV-VIS spectrometer (ULS2048, Avantes, Oude, Apeldoornseweg, Netherlands). A Deuterium-halogen light source was used to direct light towards the wafer sample at an angle normal to the surface of the wafer. The reflectance spectrum was obtained across eight (8) spots on the surfaces of each sample. This was used to characterize the homogeneity of the textured surface. The average surface roughness, R_a of the textured samples was measured using a Dektak 150 Surface profiler (Veeco Instruments Inc., Tucson, AZ, USA). R_a is the main height as calculated over the entire measured length or area. It is used to describe the roughness of the textured surfaces and detect the general variations in the overall profile height characteristics. This was used to determine the roughness profiles in six different regions across the wafers. The results from the six regions were then averaged to obtain the average surface roughness of each sample.

SEM observations of the etched wafers were carried out using a Carl Zeiss EVO MA-10 Scanning Electron Microscope that was operated at 10KV (EVO MA-10, Carl Zeiss, Hamburg, Germany). The AFM analysis of the textured surfaces used a Dimension 3100 Nanoscope IIIa Atomic Force Microscope (Bruker, Plainview, NY, USA) that was operated in the tapping mode. The AFM tips had lengths of $\sim 125 \mu\text{m}$ and tip radii of $\sim 8 \text{ nm}$. They

also had a resonance frequency of ~ 353 kHz. The scanning was done at slow scanning rates (1-3 Hz) to obtain the AFM images.

4.2.3 Solar Cell Characterization

In an effort to ascertain the effectiveness of the texturing process for light trapping scheme, simple $1 \times 1 \text{ cm}^2$ solar cell devices (with the structure of ITO/p-Si/Al) were fabricated on both textured and un-textured silicon wafers. A thin layer of ITO with a thickness of 100nm was deposited on top of the silicon substrates (as a front contact) by RF magnetron sputtering at an RF power of 50W and subsequently annealed at 250°C for 30mins. To complete the device, the Al back contact with a thickness of 150 nm was evaporated in an Edwards Auto 306 evaporator, with a vacuum better than 2×10^{-6} Torr. Following the fabrication of the devices, the illuminated I-V characteristics were measured under standard test conditions (28°C , $100\text{mW}/\text{cm}^2$) using Keithley 2400 SMU and Oriel Solar Simulator while the dark I-V characteristics for were measured without the present of light. Once the measurement was completed, the I-V parameters are obtained and plotted using Labtracer software.

4.3 Results and Discussion

4.3.1 Surface Roughness and Morphology

The dependence of average surface roughness (R_a) on etching time (t) and temperature (T) is presented in Figures 4.2a and 4.2b, respectively. The results show that R_a increases rapidly initially, with increasing etch duration. However, it becomes almost stable above the etching time of 50 minutes. Similarly, the surface roughness increases as the temperature increases. For the durations and temperature ranges investigated in this study, the highest average surface roughness value of 676 nm was obtained for an etch time of 60 minutes at an etching temperature of 90°C . The variation of R_a with t and T is attributed to

the increasing etch rate with increasing t or T . Similar trends have been reported in prior studies [13, 19].

The effects of KOH and IPA concentration (on the surface roughness) are presented in Figures 4.2c and 4.2d, respectively. These show that R_a increases with increasing KOH concentration. Similarly, the surface roughness increases with exposure to IPA. This shows clearly that both KOH and IPA concentration have a significant effect on surface roughness. Furthermore, as the proportion of IPA is increased, the resulting surface roughness is greater than that due to KOH alone (Figure 4.2d). This is consistent with prior work that suggests that IPA has a greater effect on the etching of (001)-oriented silicon wafers than KOH [13]. This can be attributed to the spreading and penetrating properties of IPA as a wetting agent, when added to alkaline etchant [28].

The SEM surface morphologies associated with the different etching durations and temperatures are presented in Figures 4.3 and 4.4, respectively. In both cases, pyramidal facets were observed on the surfaces of the (001)-oriented silicon surfaces. These are consistent with the reports from prior studies [6, 31]. They also show that alkaline etching preferentially etches {111} planes in silicon [35, 36]. At higher etch temperatures, the dimensions of the pyramids increases. Hence, for example, the pyramids formed at 90°C are larger than those formed at 70°C. They generally range in size between 2 and 10 μm as shown in Tables 4.2 and 4.3. Pyramid size is defined here as the height and base width of the pyramids that are produced on the surface of (100)-oriented silicon wafer after texturing. However, surface roughness values obtained here is dependent on this pyramid sizes and its distribution across the surface of the silicon substrate.

Furthermore, pyramidal facets were observed on the surfaces of the (001)-oriented silicon crystals that were etched with different concentrations of KOH (Figures 4.4a – 4.4d)

and IPA (Figures 4.5a – 4.5d). The densities of the pyramids also varied widely over the wafer surfaces, as shown in Figure 4.5. A high density of pyramids (approximately 80-90%) was observed on the silicon surfaces. At low volume concentrations of IPA, the silicon surfaces exhibited few large square-based pyramidal structures with increasing volume concentration of IPA. However, a further increase in the volume concentration of IPA led to a higher density of uniformly distributed pyramids with smooth pyramidal facets (Figure 4.5c). This implies that the improvement in the pyramid uniformity on the wafer can be attributed to the effects of IPA, as proposed in Ref. [13]. The SEM images of the textured surfaces also suggest that IPA has a greater effect on surface roughness than KOH.

Further evidence of the faceted etched structures was obtained from the AFM images. These were found to be qualitatively similar to the SEM images (Figure 4.3-4.5). The improved resolution of the AFM images (Figure 4.6) also revealed the non-ideal effects of etching on the surface morphologies of the etched surfaces. However, from the AFM analysis, the base angle (or facet tilt angle) of the pyramidal structures are slightly smaller compared to those produced in the case of an ideal etching where the facet tilt angle is generally accepted to be 54.74° [20, 21]. The facet tilt angles of the pyramids observed here ranges from 48° - 51° , which falls within the range specified by Baker-Finch et al. [16, 22]. A summary of the surface roughness data obtained from the AFM analysis is presented in Table 4.4. For comparison, the profilometry results are also included in Table 4.4. These show that the roughness values obtained from the AFM analyses are consistent with those obtained from profilometry.

4.3.2 Optical Reflectance and Absorbance

The dependence of the substrate optical reflectance, R , and absorbance, A , on the texturing process parameters is presented in Figures 4.7a – 4.7d and Figures 4.8a – 4.8d,

respectively. Since the optical transmittance for the 275 μm thick silicon wafers is almost zero in the visible region [37], the absorbance, A , is obtained from the expression:

$$A = 100 - R \quad (4.1)$$

The total absorbance within the textured silicon wafers, is obtained for the process parameters presented in Figure 4.8, by integrating the differential absorbance data obtained from the UV-VIS Spectrometer, over the spectrum (i.e. from 200nm to 800nm). Table 4.5 shows the total absorbance data for the different etch durations, temperatures, KOH volume concentrations, and IPA volume concentrations respectively. In all cases, the reflectance of the textured wafers was less than 10%, while the absorbance was greater than 90%. For exposure durations of up to 40 minutes (Figure 4.7a), the effects of etching time were found to be very limited. However, for durations up to 60 minutes, the reflectance decreased with increasing exposure to alkali etchants. Similar trends have been reported by Mackel [32] and Llopis *et al.* [38], for anisotropically-etched single crystal (001) silicon wafers.

The effect of etching temperature on the optical reflectance is presented in Figure 4.7b. This shows that the reflectance decreases initially, for wavelengths between 230 nm and 400 nm, as the etching temperature increases between 60°C and 80°C. For wavelengths within the visible spectrum (400 nm-700 nm), the reflectance decreases continuously, as the etching temperature increases from 60°C to 80°C.

However, above 80°C, increasing temperature is associated with similar reflectance at 80°C. This is attributed to the faster dissolution kinetics, as suggested in prior work by Allongue *et al.* [39]. The effects of KOH: IPA ratios on the optical reflectance are presented in Figures 4.7c and 4.7d. These results show that IPA has a greater effect on the surface reflectance than KOH. This is consistent with prior results obtained from the etching of (001)-oriented silicon wafers [38, 39].

4.3.3 I-V Characteristics

Figures 4.9a and 4.9b present the dark I-V characteristics and illuminated I-V characteristics respectively. As expected, the dark I-V curve produced a diode like nature for both the textured and untextured substrates (see Figure 4.9a). To provide a basis for comparison, the solar parameters were obtained under light. The result from Figure 4.9b shows that the solar device with a textured substrate had a fill factor, FF of 0.47, short circuit current, I_{sc} of 0.189mA and a maximum power, P_{max} of $3.83 \times 10^{-5}W$ while the solar device with an untextured substrate had a FF of 0.50, short circuit current, I_{sc} of 0.158mA and a maximum power, P_{max} of $3.00 \times 10^{-5}W$.

The measured short circuit current, I_{sc} for the textured solar device is found to be higher compared to the solar device with untextured substrate. The results show that the texturing provides a clear boost to the current, by slightly more than 0.03mA. Unexpectedly, the fill factor, FF is found to be relatively higher for the solar device for the untextured substrate compared to that fabricated with textured substrate. This effect could be the result of a lower resistive contact of the ITO film deposited on the macroscopic rough surface. Moreover the gap in P_{max} can be traced back to a better I_{sc} of the textured cells.

4.3.4 Implications

The implications of the above results are quite significant. They show that IPA concentration has a greater effect on surface roughness than the effect of KOH concentration (Figures 4.2 and 4.7). Higher volume concentrations of IPA result in rougher surfaces and more uniform distributions of pyramids. They also increase the densities of pyramids on the silicon surfaces. However, the variations in pyramidal texture from rough to smooth facets (shown in Figure 4.5) can also be attributed to the effect of increasing volume concentration of IPA. This leads to a decrease in reflection shown later in Figure 4.7d.

The above results suggest that the ratio of IPA concentration to KOH concentration can be tuned to control the etching of (001) silicon surfaces and the final surface morphology. Ultimately, this insight can be used to control the wafer surface reflectance of silicon wafers. The etch rate can also be accelerated by increasing the etch temperature and duration, as shown in Figures 4.2 and 4.7. However, etch temperatures above 80°C should be avoided since this is above the boiling point of IPA (~82.4°C) [40]. Etching at higher temperatures can also initiate cracks in the silicon wafer, as shown in Figure 4.4d. Evidence of temperature-induced cracking has also been presented by C. Sethi *et al.* [41] for silicon wafers subjected to temperature greater than 80°C.

The AFM images also revealed the occurrence of some local roughening or damage of the {111} facets, after etching with higher KOH concentrations (Figures 4.6c and 4.6d). Such local roughening may lead to damage and light scattering. There is, therefore, a need to limit the concentration of KOH to levels that can minimize such local roughening. In contrast, the etching (001)-oriented silicon surface is enhanced by increasing the concentration of IPA in a moderate concentration of KOH. When this is done, the surface roughness increases with increasing IPA concentration (Figure 4.2d). These results lower surface reflectance over the range of wavelengths that is relevant to (001)-oriented single crystalline silicon solar cells. This reduced reflectance enables more light to be trapped for the photo-conversion of light into charge. It can, therefore, be used to enhance the optical absorbance and efficiency of the c-Si solar cells from 63% to 87% [31] and 12.5 to 25.6 [7, 31] respectively.

Finally, without considering the details of the device efficiency, the solar parameters obtained from Figure 4.9b show that there is a slight difference between the solar device with textured substrate and that with untextured substrate. Moreover, it would be expected that this relative difference in the short circuit current would become even greater after increasing the device area and adding a silver grid to the device configuration. However, it is clear that

further work need to be done by fabrication more solar cells in a more ideal situation and environment.

4.4 Conclusions

In this chapter, the effects of KOH: IPA etching of (001)-oriented silicon single crystals is explored. The results show that IPA concentration has a greater effect on the surface roughness of (001)-silicon single crystals at temperatures up to 80°C. The etch rate also increases with increasing etching temperature/duration and increasing concentration of KOH. However, the volume concentrations of KOH: IPA above 2:4 can give rise to surface damage after exposures of ~ 1 hour. Increasing volume concentration of IPA also results in smoother pyramidal facets on (001)-oriented silicon surfaces.

The reductions in surface reflectance associated with controlled etching of (100)-oriented silicon wafers with KOH: IPA mixtures suggest that the controlled etching can be used to trap light by the formation of textured silicon surfaces that promote multiple reflections. The increased interactions with incident light rays can enhance the amount of light absorbed by (001) silicon single crystals. Hence, the controlled texturing of silicon wafers can be used to enhance the absorbance and photo-conversion efficiencies of (100)-silicon solar cells by reduction of the reflectance. The solar parameters discussed above show that there is a slight evidence of the enhancement especially with the short circuit current obtained for the solar device fabricated with the controlled textured substrate

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Table 4.1: Summary of experimental conditions

Step	Process	Chemicals	Details
1	HF-Dip	0.5:100, HF-Dip:DI	25 ⁰ C, 100secs
2	Anisotropic etching	Etchant concentration (V/V %)	40% KOH:IPA:DI H ₂ O
		Etch time (Minutes)	30, 40, 50, 60
		Etch temperature (⁰ C)	60, 70, 80, 90
3	Rinsing	DI	25 ⁰ C
4	Drying	Stream of dry N ₂ gas	

DI H₂O: Deionized Water, 18MΩ.cm, HF: 0.5% Solution

Table 4.2: Variation of pyramid size on silicon textured surface at different etch temperature

Process Parameter [Temperature(⁰ C)]	Average Pyramid Size (μm)	Remarks
60	2.75	Small Non-uniform
70	5.33	Medium Low density
80	6.91	Medium High density
90	10.8	Big Non-uniform

Table 4.3: Variation of pyramid size on silicon textured surface at different IPA concentration

Process Parameter [IPA Concentration (g/ml)]	Average Pyramid Size (μm)	Remarks
KOH: IPA: DI		
2 : 1 : 46	2.37	Small Non-uniform
2 : 2 : 46	3.78	Small Non-uniform
2 : 4 : 46	6.4	Medium Uniform
2 : 8 : 46	10	Big Uniform

Table 4.4: Summary of surface roughness data

Process Parameter	Profilometry Average Roughness (R_a)	AFM Localized Roughness
	(nm)	(nm)
Etch time (Minutes)	30	201
	40	565
	50	621
	60	643
Etch temperature (Degrees)	60	342
	70	574
	80	641
	90	676
IPA concentration (g/ml)	1	315
	2	529
	4	604
	8	681

Table 4.5: Total absorbance data (integrated over the spectrum) for textured silicon wafers at different (a) etch times (b) etch temperatures (c) KOH volume concentrations and (d) IPA volume concentrations.

a			b		
Process Parameter		Total Absorbance (%)	Process Parameter		Total Absorbance (%)
Etch time (Minutes)	30	95.34	Etch temperature (Degrees)	60	93.03
	40	95.26		70	94.49
	50	96.20		80	95.34
	60	97.07		90	94.71

c			d		
Process Parameter		Total Absorbance (%)	Process Parameter		Total Absorbance (%)
KOH Concentration (g/ml)	1	94.13	IPA Concentration (g/ml)	2	95.13
	2	95.76		4	95.76
	4	95.15		8	97.32

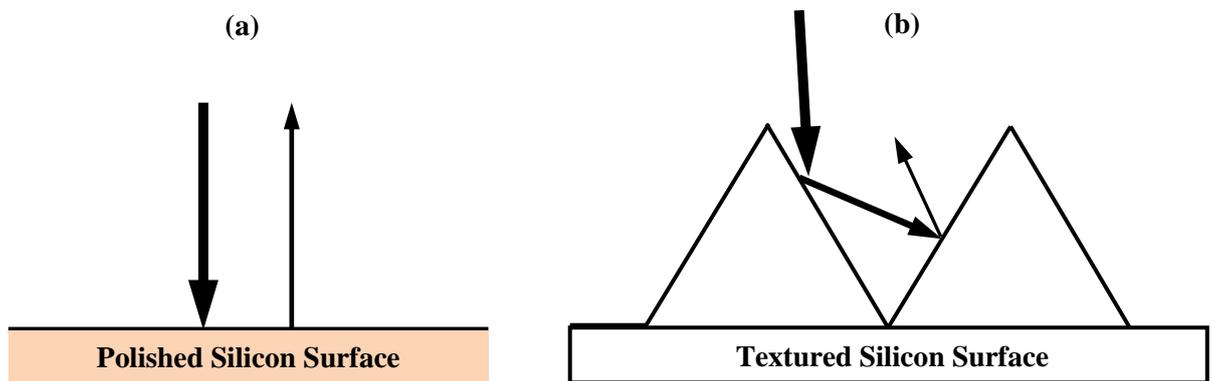


Figure 4.1: Schematic of light interactions with silicon surfaces: (a) Reflection loss on polished silicon surface; (b) Minimizing reflection loss on textured silicon surface.

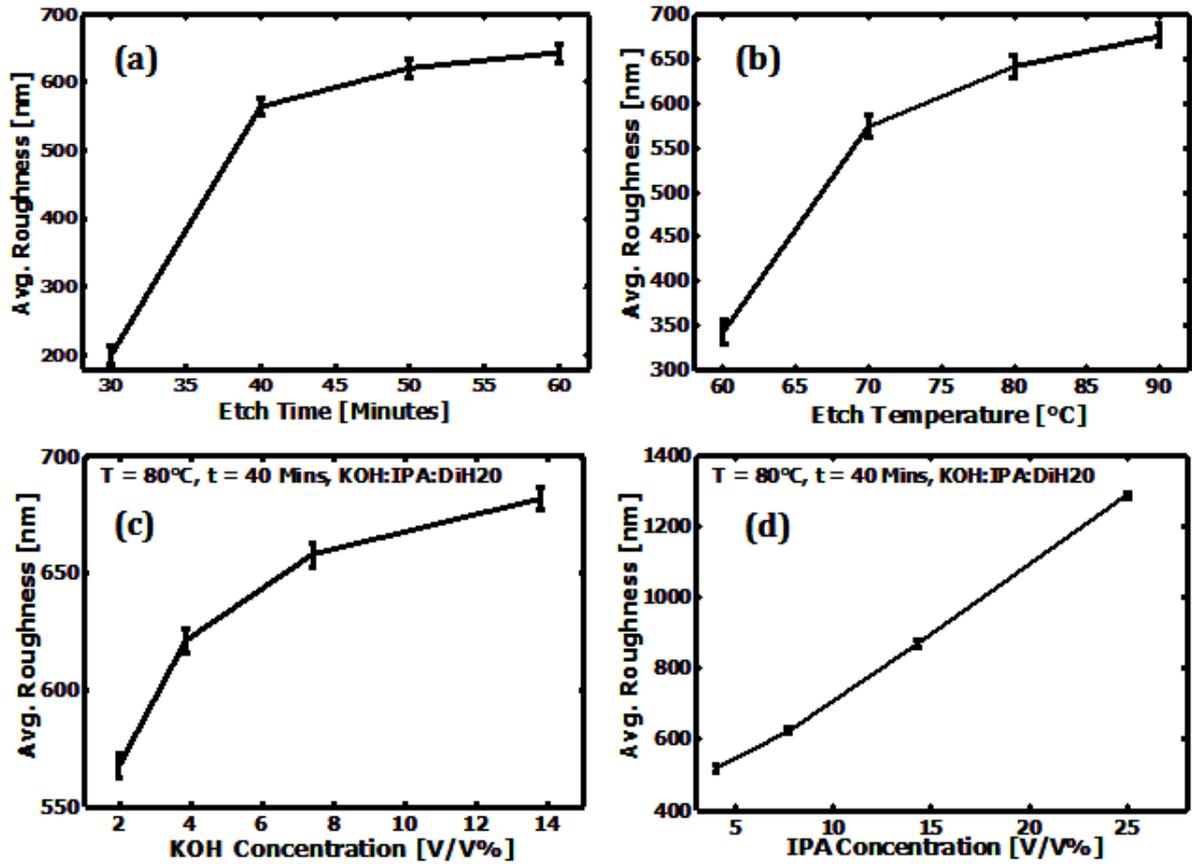


Figure 4.2: Average roughnesses data for textured (001)-oriented wafers at different (a) etch time (b) etch temperature, (c) KOH volume concentrations and (d) IPA volume concentrations.

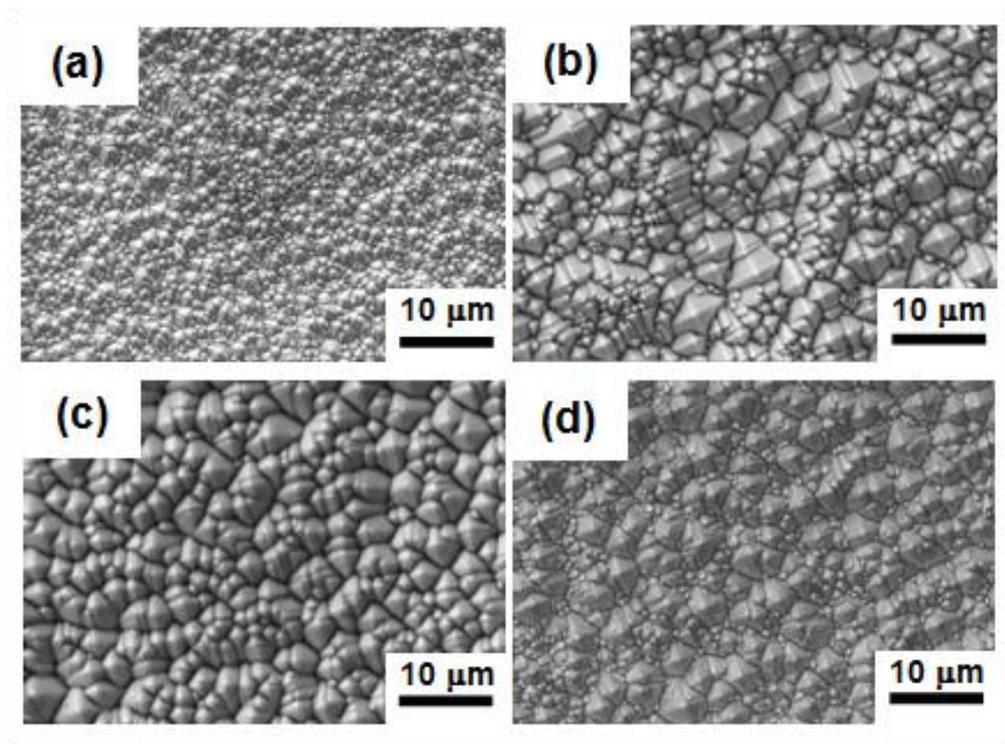


Figure 4.3: SEM images of the textured (100) wafers for (a) 30 min, (b) 40 min, (c) 50 min and (d) 60 min.

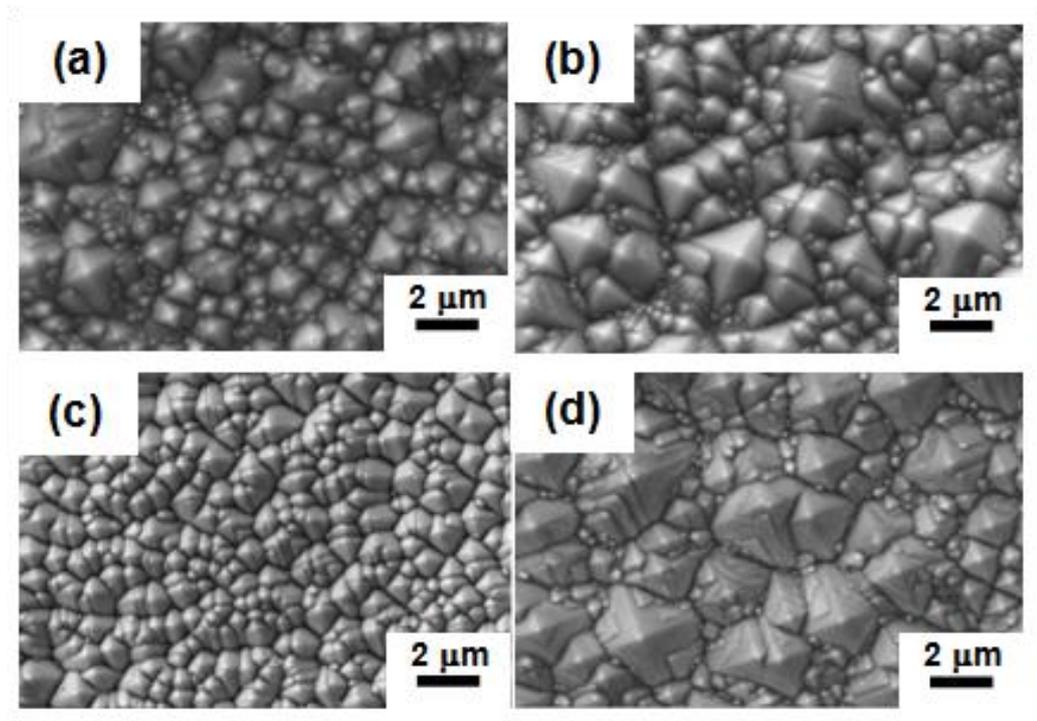


Figure 4.4: SEM image at higher magnification showing a pyramidal coverage obtained on textured (100) wafer samples at (a) 60⁰C (b) 70⁰C (c) 80⁰C and (d) 90⁰C.

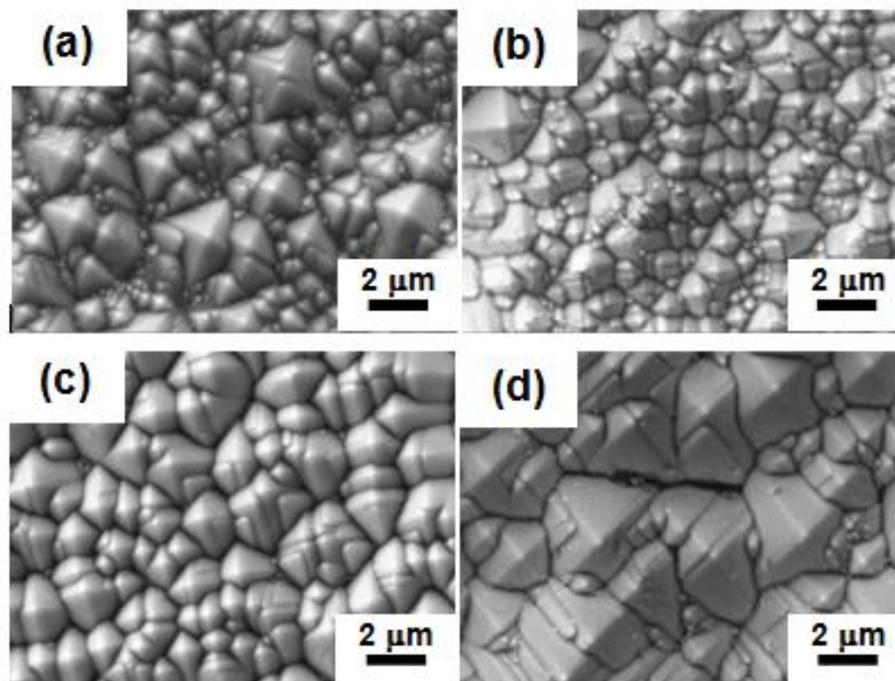


Figure 4.5: SEM image at higher magnification showing a pyramidal coverage obtained on textured (100) wafer samples at different IPA concentration.

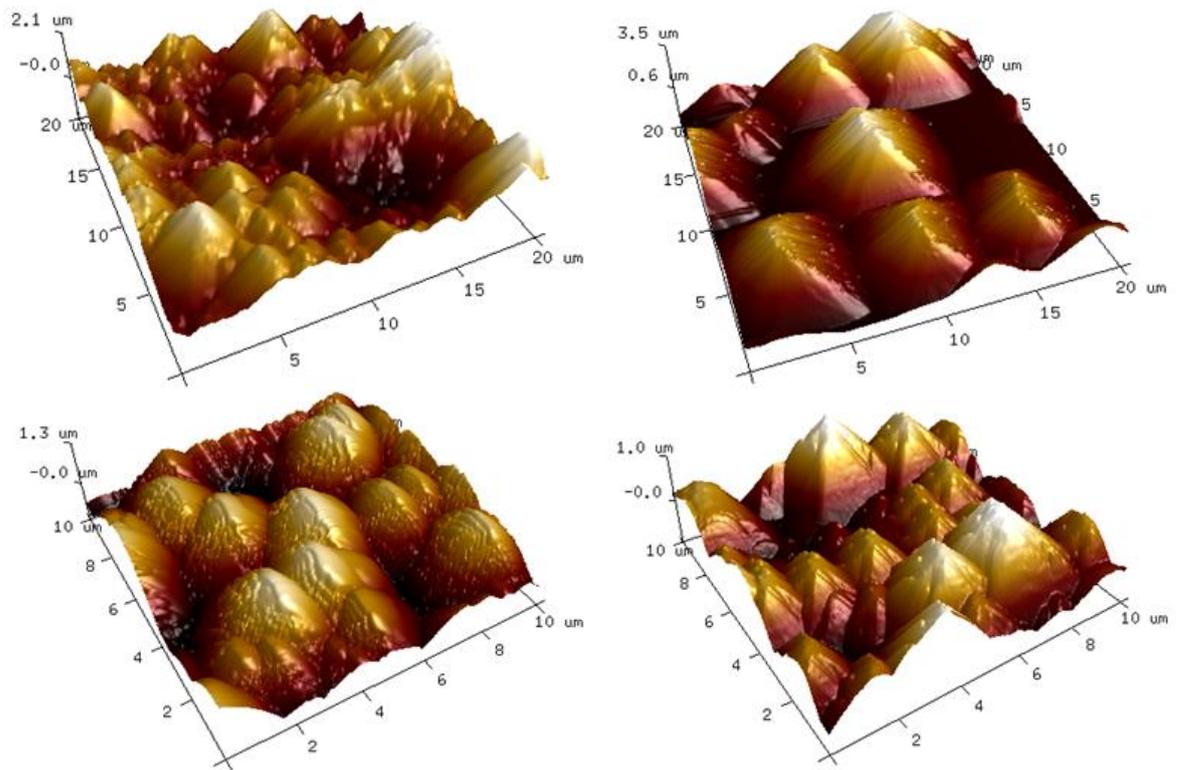


Figure 4.6: 3D profile AFM images of KOH textured silicon wafer samples at different IPA.

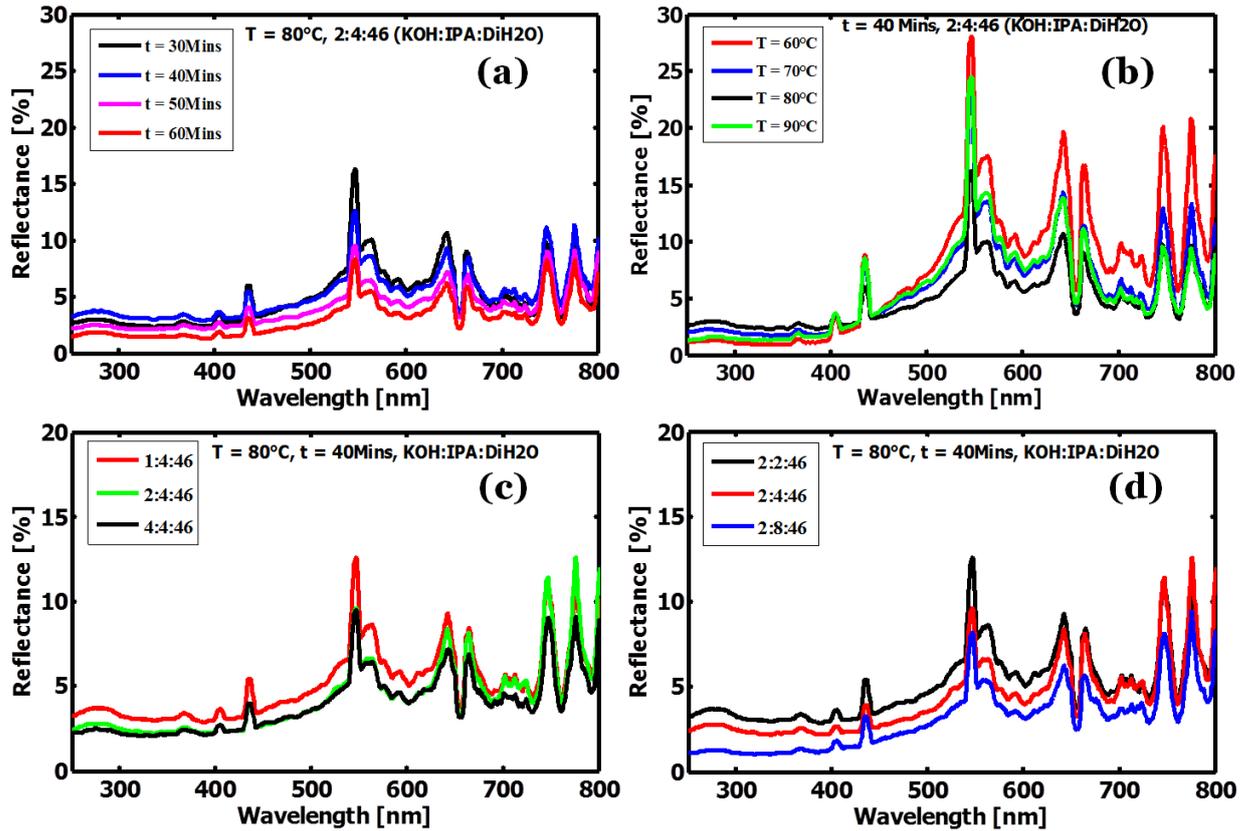


Figure 4.7: Reflectance spectra of textured wafers at different (a) etching time (b) etch temperature (c) KOH volume concentrations and (d) IPA volume concentrations.

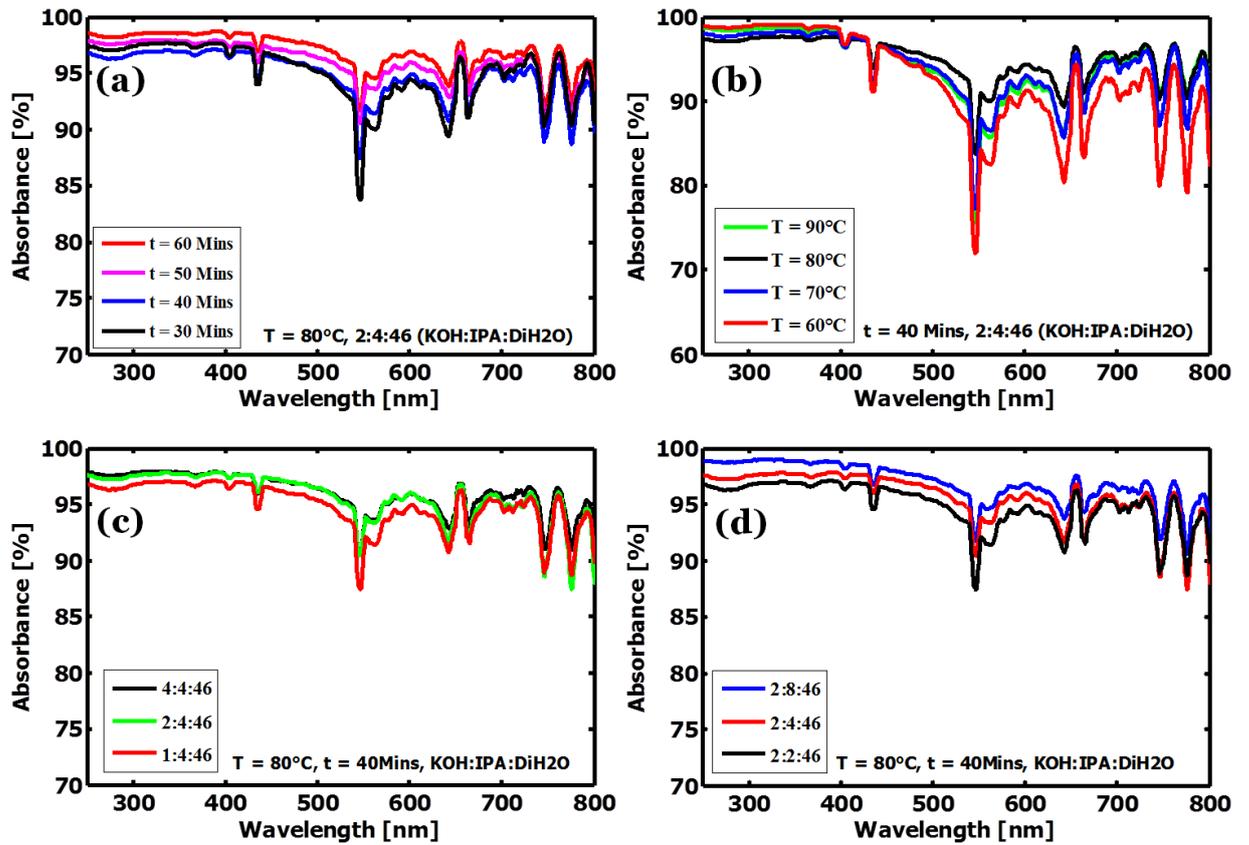


Figure 4.8: Absorbance spectra of textured wafers at different (a) etching time (b) etch temperature (c) KOH volume concentrations and (d) IPA volume concentrations.

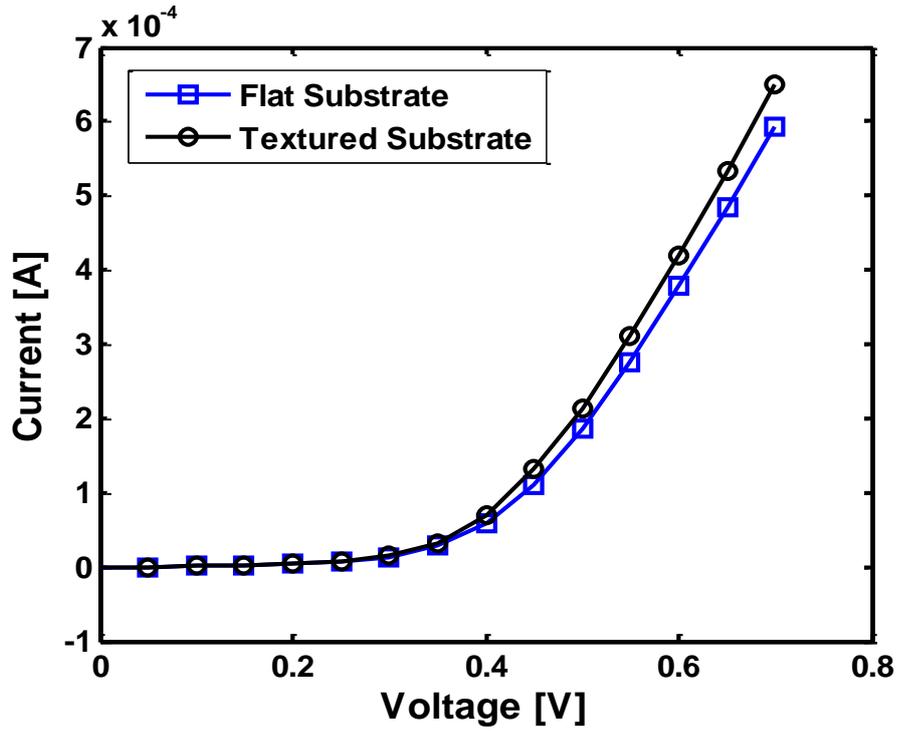


Figure 4.9a: Current-Voltage (I-V) characteristics of a p-n Junction Solar cell device in the Dark.

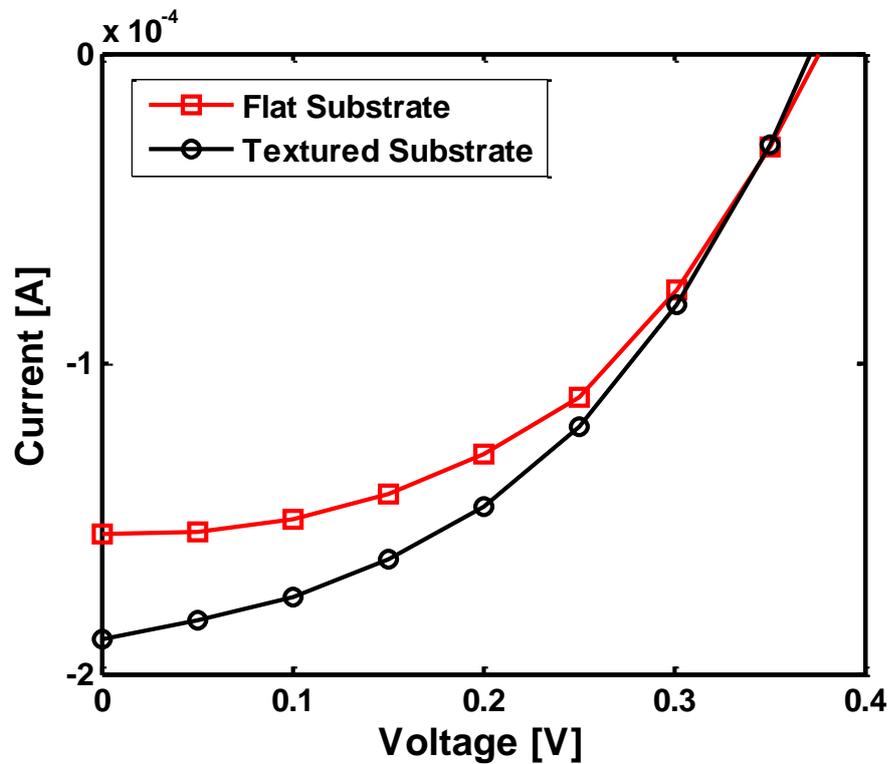


Figure 4.9b: Current-Voltage (I-V) characteristics of a p-n Junction Solar cell device in the Light.

CHAPTER FIVE

MODELING OF FATIGUE FAILURE IN SILICON MEMS STRUCTURES

5.1 Introduction

The interest in the application of micro-electro-mechanical-systems (MEMS) [1-3] has led to the introduction of a variety of commercial products (medical and computer devices) into the marketplace. These applications include: biological sensors in the human body, hydrostats, pressure sensors, inertial sensor, ink jet cartridge nozzles, pressure transducers, linear racks, accelerometers and actuators [1-3]. The suitability and success of silicon in micro-machining technology has made it the material of choice in most MEMS applications [4]. However, the reliability of the resulting devices is dependent on the type of loading and the environmental conditions [5].

In particular, in the case of materials that are used for the safety-critical applications, the application of cyclic loads can lead to “fatigue” failure at stresses that are well below the fracture strength under monotonic loading. The incidence of fatigue failure can also be exacerbated by the combined effects of chemical environments (especially water vapor) and mechanical loading [5]. There is, therefore, a need for models that can predict the combined effects of environment and mechanical loading on the fatigue failure of silicon MEMS structures.

Fatigue failure involves the nucleation and growth of cracks under cyclic loading conditions at stresses below the strengths obtained under monotonic loading [5-7]. It accounts for about 90% of all failures in engineering components and systems [6, 7]. However, although the mechanisms of fatigue have been studied extensively in bulk materials since the industrial revolution in the 19th century [5], our current understanding of the fatigue of bulk silicon and silicon MEMS thin films is limited to the results from studies that have been performed over the past few decades [8-19].

In the case of bulk silicon, it has been shown that crack nucleation and growth do not occur under static or cyclic loading conditions [8-10]. Hence, it was surprising for many when Connally and Brown presented experimental evidence of fatigue in silicon MEMS thin films in 1992 [4]. Their studies revealed that micron-sized silicon structures failed prematurely in air at room-temperature (approx. 25°C) under cyclic loading conditions. They obtained stress-life and sub-critical fatigue crack growth rate data that suggested a strong influence of water vapor on the fatigue of silicon MEMS structures. Their findings have been validated by many other studies [11-19] that have been carried out on the fatigue behavior of both single crystal [20] and polycrystalline silicon MEMS thin films/structures [21].

Like Connally and Brown [4], other researchers used silicon MEMS specimens that were fabricated by silicon micromachining technology that enabled external [22] and integrated [23, 24] cyclic loading. Prior work on the fatigue of silicon has also resulted in a number of empirical models and insights for the prediction of fatigue in silicon MEMS structures [18, 21-26]. The results from these studies suggest that: an increase in high-cycle fatigue lifetime occurs with decreasing peak stress [25]; the fatigue life depends on the cyclic stress levels, but not on cyclic frequency [22]; morphological changes in the surface silica occur during fatigue [26]; and surface cracks may grow in the top oxide film due to slow crack growth mechanisms [19].

Nevertheless, in spite of the extensive research that has been performed on silicon MEMS structures, there is still no consensus on the mechanisms of fatigue crack nucleation and growth in silicon MEMS structures [27]. Some researchers suggest that silicon MEMS fatigue occurs due to the growth of surface perturbations until they evolve into cracks (Figure 1a) [18, 19]. In this case, the topical oxides also appear to thicken during cyclic loading, (Figure 1a) [27-29]. Other groups suggest that cracks formed during fabrication can extend by slow crack growth via stress- and environmentally-assisted oxide thickening, when the

crack driving force exceeds a critical value (Figure 1b and 1c) [19, 21, 25], while others suggest that sub-critical growth occurs due to a mechanical fatigue mechanism [12]. There is, therefore, a need for further work to establish the mechanisms of fatigue in silicon MEMS structures.

Since the initiation of cracks represents a significant fraction of the fatigue life in silicon MEMS structures [18], this chapter explores the effects of stress and environmentally-induced evolution of the roughness of the topical oxide film due to stress, temperature and environmentally-enhanced dissolution mechanisms [15, 17]. Analytical and computational models are used to study the role of the stress-assisted dissolution of the topical SiO₂ layer that is observed on the surfaces of silicon MEMS structures. The possible evolution of the thin SiO₂ layer is simulated and compared with measured surface profiles from prior work [26]. The possible formation and growth of cracks is elucidated before discussing the micro-mechanisms of fatigue fracture.

5.2 Stress-Assisted Dissolution Model

When a stressed solid material comes in contact with an environment (vapor or liquid solution) it may gain from or lose mass to its environment. However, the dissolution rate is dependent on stress and as a result of the stress-assisted dissolution, the elastic energy adds to the driving force of the reaction, and may cause the surface to roughen. Stress is also known to change the mobility of a reaction. The surface reaction is driven by interfacial and elastic energy and by chemical potential difference between the solid and its environment.

In the case of silicon MEMS thin films/structures, stress-assisted dissolution has been suggested as a possible mechanism for crack nucleation [30, 31]. However, the dissolution reaction is influenced by both surface energy and strain energy of the stressed surface. An early study by Mullins [32] in 1957 indicates that when a solid is perturbed into a wavy

shape, the surface energy causes the solid to evaporate faster at the crests than at troughs, so that the wave amplitude decays over time, and the surface flattens.

Following the work done by Mullins [32], Srolovitz [33] established that when stress is applied to the wavy surface a non-uniform stress field is induced (the magnitude of the stress is larger at troughs than at crests). Consequently, the solid evaporates faster at the troughs than at crests, so that the wave amplitude grows over time and the surface roughens. However, when both the surface energy and stress act together, the ratio of the surface energy to the elastic energy defines a length scale: shorter wavelengths decay, while longer wavelengths grow.

Kim et al. [34] and Yu and Suo [31] have used linear perturbation analysis to study the dissolution of a stressed solid surface and the related changes in the surface profile to the stress state. They compared experimental profiles with those predicted by an idealized kinetic law. A similar analysis is used here to study the observed roughening of the SiO₂ layer on the silicon MEMS structure.

5.2.1 Surface Dissolution Reaction Model

Following the work of Yu and Suo [31], we consider a silicon MEMS structure to be in contact with an environment. The mobility within the environment is large enough to make the chemical potential uniform. However, the SiO₂ layer and the environment are not in equilibrium with each other since the SiO₂ layer loses mass to the environment by dissolution. Thus, as the surface reaction proceeds, the SiO₂ environment (as a system) reduces its total free energy (G).

The total free energy consists of the surface energy(U_S), the grain boundary energy(U_B), the chemical energy(U_C), the elastic energy(U_E), and a term U_L due to the applied traction. This can be expressed as:

$$G = U_S + U_B + U_C + U_E - U_L \quad (5.1)$$

Since the SiO₂ layer and the environment are not in equilibrium with each other, the free energy variation associated with unit volume of the SiO₂ layer grown on the surface of the surface of the silicon MEMS does not vanish. Rather, it defines a driving force of the dissolution reaction for the SiO₂ layer under a state of stress and with a curved surface. The driving force, F is thus expressed as [31]:

$$F = g - w - K\gamma \quad (5.2)$$

Here g is the free energy difference between the atoms in two bulk phases (i.e., the environment and the unstressed solid), w is the elastic energy per unit volume, γ is the surface energy per unit area and K is the sum of principal curvatures. The SiO₂ layer gains mass when $F > 0$, and loses mass when $F < 0$.

The reaction rate, R , i.e. the volume of SiO₂ layer gained or lost per unit surface area per unit time, is a function of the driving force, F . R is assumed to vary linearly with the driving force. Thus, the linear kinetic law is adopted here for simplicity [34]:

$$R = MF \quad (5.3)$$

The proportionality constant M is known as the mobility of the surface. Since surface reaction is a thermally activated process, M depends on temperature and the mobility may follow the Arrhenius relation [31]:

$$M = M_0 \exp(-Q/kT) \quad (5.4)$$

where k is Boltzmann's constant, and T the temperature. The activation energy Q and the pre-exponential factor M_0 are parameters to fit experimental data. We assumed that the mobility M is independent of the applied stress.

The linear kinetic law in Equation (5.3) is, however, a special case of a more general law introduced by Hillig and Charles [35] in 1965. It is valid when the driving force is small compared to the average thermal energy.

5.2.2 Film Roughening and Evolution

5.2.2.1 Linear Perturbation Analysis of Stress-Assisted Dissolution

When the SiO₂ layer interacts with an environment (vapour or liquid solution), we assume it is subject to a uniform biaxial stress field, σ , and remains elastic. In order to highlight the effect of the stress state, the SiO₂ layer is considered to be isotropic and homogeneous, with Young's modulus, $E=72GPa$ [29, 36] and Poisson's ratio $\nu=0.22$ [36], and always in mechanical equilibrium. However, for the surface to change shape for each time step, Equations (5.2) and (5.3) determine the reaction rate. Thus, the reaction rate, R , is given by [34]:

$$R = \frac{\partial H}{\partial t} = M(g - w - K\gamma)\sqrt{1 + |\nabla H|^2} \quad (5.5)$$

where H is the height of the SiO₂ surface and ∇ represents the 2-D gradient operator.

Since the SiO₂ layer is subjected to a uniform biaxial stress, the height, $H(x, t)$, of the surface is decomposed into the average height $\langle H(x, t) \rangle$, and the surface roughness, $h(x, t)$ such that:

$$h(x, t) = H(x, t) - \langle H(x, t) \rangle \quad (5.6)$$

By adopting the experimental data obtained by Shrotriya et al. [26] for the vertical distance between the highest and lowest points on AFM selected line scans, Equation (5.6) can be used to compute the surface roughness of the SiO₂ layer. The curvature of the surface can be approximated as $K \propto \nabla^2 h$ when $|\nabla h| \ll 1$, thus the first-order evolution of the surface roughness can be expressed as:

$$\frac{\partial h}{\partial t} = M\{\gamma \nabla^2 h + \Delta w\} \quad (5.7)$$

where $\Delta w = w - w_0$.

Likewise, when the SiO₂ layer is subjected to in-plane stress state (Figure 5.2) with principal stresses σ_1 & σ_2 and principal axis x_1 & x_2 , the height, $H(x_1, x_2, t)$ of the surface

is decomposed into the average height $H_0(t)$ and the surface roughness, $h(x_1, x_2, t)$ such that:

$$H(x_1, x_2, t) = H_0(t) + h(x_1, x_2, t) \quad (5.8)$$

Now, to study the time evolution of the SiO₂ surface roughness, the roughness of the surface is seen as a linear superposition of the Fourier components, $q(\omega, t)$ of wave vectors (lying in $x_1 - x_2$ plane) of all magnitudes and directions. So that, when the wave amplitude is small, to the first order in wave amplitude, the time evolution of one Fourier component is independent of another. Thus, only one Fourier component needs to be analyzed. Figure 5.2 illustrates a wave vector of magnitude ω pointing in the direction x which is at an angle θ from the x_1 axis. The two components of the wave vector are $\omega_1 = \omega \cos \theta$ and $\omega_2 = \omega \sin \theta$. Thus, we assume that the roughness has one single Fourier component, which is a cosine-wave in the x direction:

$$h = q(\omega, t) \cos \omega x \quad (5.9)$$

Here, the wave amplitude is assumed to be small compared to the wavelength namely, $\omega q \ll 1$ for the linear perturbation analysis to be performed. Then, the Fourier component $q(\omega, t)$ is considered a small perturbation and results are retained up to the leading term in the wave amplitude q . To the leading order in q , the reaction rate is [31]

$$R = \frac{dH_0}{dt} + \frac{\partial h}{\partial t} \quad (5.10)$$

Similarly, the driving force, F , to the leading order in q is obtained as [31]:

$$F = F_0 + \alpha h \quad (5.11)$$

where F_0 is the driving force for an perfectly flat surface subjected to the principal stresses σ_1 and σ_2 . While α is expressed in terms of stress state and material properties as:

$$\alpha = \frac{2(1 + \nu)}{E} [(1 - \nu)(\sigma_1 \cos^2 \theta + \sigma_2 \sin^2 \theta)^2 + (\sigma_1 - \sigma_2)^2 \cos^2 \theta \sin^2 \theta] \omega - \gamma \omega^2 \quad (5.12)$$

where, E and ν are the Young's modulus and Poisson's ratio of the material, respectively.

By relating Equations (5.3), (5.10) and (5.11), it can be concluded that:

$$\frac{\partial h}{\partial t} = M \alpha h \quad (5.13)$$

By integrating Equation (5.13) with respect to time, we obtain the expression [31]:

$$\ln \frac{q(\omega, t)}{q(\omega, 0)} = M \alpha t \quad (5.14)$$

Hence, when the quantity, α , is positive, amplitudes of the corresponding wavelength grows with time and when it is negative the amplitude of wavelength decays with time. The quantity, α , corresponding to stress state at base of the notch, is evaluated for the different Fourier components in order to study the influence of the stress-assisted surface reaction. In order to identify the Fourier components with amplitudes that grow with time, fast Fourier transforms of the surface morphologies (before and after actuation) is obtained from [36] according to Equation (5.12) and the surface profile is then represented by the Fourier transform [36]:

$$h(x_1, x_2, t) = \int q(\omega_1, \omega_2; t) \exp i(\omega_1 x_1 + \omega_2 x_2) d\omega_1 d\omega_2 \quad (5.15)$$

where ω_1 & ω_2 are wave numbers.

5.2.3 Oxide Thickening

As stated in section II, the SiO₂ layer is considered here to be linearly elastic, isotropic and homogeneous so that the potential role of the surface oxide films in the fatigue behavior of Si MEMS can be modeled. The model considered the fracture mechanics framework for the crack tip in thickening SiO₂ layer. Following the suggestion by Muhlstein et al. [25] that

the thickening of SiO₂ layer occur during cyclic actuation of Si MEMS structures, the energy release rate, G associated with the crack tip in the SiO₂ film layer, can be estimated from the following expression [36]:

$$G_0 = \frac{\sigma_f^2 h \omega}{E_f} \quad (5.16)$$

where σ_f is the stress in the oxide layer; h is the oxide layer thickness; $E_f^* = E_f/(1 - \nu)$; E_f and ν are the Young's modulus and Poisson's ratio of the oxide layer, respectively; ω is the dimensionless factor depending on the crack length, film thickness, and elastic properties of the film and substrate. When the crack-tip is inside the oxide layer for this particular geometry, ω is given by the expression [36]:

$$\omega = 3.951 \left(\frac{a}{h}\right) \left[1 - \frac{a}{h}\right]^{1-2s} \left[1 + \lambda_1 \left(\frac{a}{h}\right)\right]^2 \quad (5.17)$$

Here, a , is the crack size; λ_1 is a fitting parameter to the full numerical solution tabulated in Ref. 36 and the coefficient, s , is chosen such that as $a/h \rightarrow 0$ Equation (5.17) approaches the classical solution of an edge crack in a semi-infinite homogenous plane [36].

For a crack that penetrates into the substrate ($a > h$), ω is given by the expression [36]:

$$\omega = \frac{4\pi}{\pi^2 - 4} \left(\frac{E_f^*}{E_s^*}\right) \left(\frac{a}{h}\right) \left[\sin^{-1} \left(\frac{h}{a}\right) \left(1 - \frac{h}{a}\right)^{1/2-s} \left(1 + \lambda_2 \left(\frac{h}{a}\right)\right) \right]^2 \quad (5.18)$$

where, λ_2 is a fitting parameter; $E_s^* = E_s/(1 - \nu)$; E_s and ν are the Young's modulus and Poisson's ratio of the substrate, respectively.

In cases where the crack-tip extends along the interface, ω is given by the expression [36]:

$$\omega = \frac{1}{2} \left(\frac{a/h}{1 + (a/h)} \right)^{1-2s} \left[1 + \lambda_3 \exp \left(-\lambda_4 \sqrt{\left(\frac{a}{h} \right)} \right) \right] \quad (5.19)$$

where, λ_3 and λ_4 are the fitting parameters that can be interpolated from the values tabulated in Ref. 36 and the coefficient, s , in this case ensures that the solution of Equation (5.19) is exact as $a/h \rightarrow \infty$.

5.3 Finite Element Modeling

5.3.1 Crack Growth and Failure

In an effort to examine the regimes in which crack growth can occur, the linear elastic fracture mechanics framework described in section 5.2.3 is used to identify the conditions for stable and unstable crack growth in the SiO₂ layer. Finite element analyses (FEA) was performed in ABAQUS 6-9 (ABAQUS, Dassault, Systemes International, Pawtucket, RI). The FEA approach relied on the finite element (FE) calculation of the stress/strain distributions, energy release rates, and the stress intensity factors of cracks in the SiO₂ layer.

In the calculations, material properties including E and ν were assigned with a section thickness of 19.5 μm for the substrate and 0.1 μm for the oxide films. The Young's modulus was taken as $E = 169 \text{ GPa}$ for silicon MEMS [37] and $E = 72 \text{ GPa}$ for the SiO₂ film [29, 36] respectively. The Poisson's ratio was taken as $\nu = 0.22$ for silicon MEMS [37] and $\nu = 0.22$ for the SiO₂ film [36].

A pressure load was then applied to the sides of the silicon MEMS structure to simulate a uniform nominal axial stress. Mesh refinement was carried out until the elastic energy converged. The mesh was concentrated at the crack tip, since we were interested in the total stored elastic energy for each crack length. A focused meshing strategy was used to increase the number of elements in the vicinity of the crack-tip that required a partitioning scheme.

Both plane stress and plane strain cases were considered. The total force required at each displacement step is determined and compared with experimental data for the associated crack length. Once the axial load of the model has been correlated with experiment, the energy release rate is recorded and plotted against the crack length. The ABAQUS software was used to determine the J-integral values using contour integrals.

5.4 Results and Discussion

5.4.1 Film Roughening and Evolution

In To study the influence of the stress-assisted surface reaction, the quantity, α , corresponding to stress state at base of the notch was evaluated for the different Fourier components. Since the value of the quantity, α , is only influenced by the magnitude of the stress field, the root-mean-squared (RMS) average of the principal stresses was used in the calculations. This was done in order to account for cyclic loading. The RMS average of principal stresses and the stress state values employed in the calculations were obtained from Refs. [29, 38].

The RMS average of the in-plane stresses at the base of the notch has been computed to be $\sigma_{11} = 1990$ MPa, $\sigma_{22} = 141$ MPa and $\sigma_{12} = 0$ [29]. Also, the interfacial energy of the SiO₂ and water system has been reported to be 4.8 J/m² [38]. These values were substituted in Equation (5.12) in order to express α as a function of Fourier components of the surface roughness. The quantity on the left-hand side of Equation (5.13) represents the evolution of Fourier components of surface roughness with time. The contour plot of α corresponding to the stress state is presented in Figure 5.4. The dark thick contour line on the plots corresponds to $\alpha = 0$, and $\alpha > 0$ for all of the wave numbers enclosed by it.

Following the procedure described by Kim et al. [34], Shrotriya et al. [26, 29] used the AFM measured surface topologies of the MEMS structure to determine the

$\ln q(\omega, t)/q(\omega, 0)$ (from 5.14 Equation) that corresponds to an area of $2 \mu\text{m} \times 2 \mu\text{m}$ near the notch-tip (see Figure 5.5). Comparison of the contour plots of $\ln q(\omega, t)/q(\omega, 0)$ and α indicates that the shape of the contours is similar. Moreover, the magnitude of wave numbers predicted to grow by linear perturbation analysis, compares remarkably well the experimental measurements carried out by Shrotriya et al. [26, 29] (see Figure 5.5).

To quantify the extent of change in the topography of the Si MEMS structure as a function of distance from the bottom of the notch, data for the vertical distance between the highest and lowest points on AFM selected scan profiles were obtained from Ref. [24, 29]. The roughness information from the scan lines was taken progressively from the surface of the sample at regular intervals. Equation (5.6) was then used to compute the surface roughness, $h(x, t)$ of the SiO_2 layer.

Figure 5.6 shows the computed surface roughness parameter $h(x, t)$ plotted against the distance from the bottom of the notch. It can be deduced that, during actuation, the surface roughness changes significantly with increasing distance from the bottom of the notch. However, the regions that are closer to the bottom of the notch of the actuated surface are resulted in much higher surface roughness values (see Figure 5.6). This clearly shows the effects of stress on the evolution of surface topography under cyclic loading. The result also suggests that the surface topography evolution is associated with the roughening of the SiO_2 film that is present on the surface of the silicon MEMS substrate.

Figure 5.7 shows the AFM images from the work of Shrotriya et al. [24]. Figures 5.7a and 5.7b present the AFM image before and after actuation for 12.79×10^9 cycles, respectively, while Figure 5.7c is the subtracted image that shows the extent of change in the surface topography during actuation of the MEMS structures. The image shows a clear increase in the surface roughness at the bottom of the notch, where the highest cyclic stresses exist. The increase can best be observed by comparing Figure 5.7b with Figure 5.7c and then

relating it to Figure 5.6. This clearly demonstrates the effect of stress on the evolution of surface topography under cyclic loading. However, a comparison of the results presented in Figure 5.6 with those presented by Shrotriya et al. [24] in Figure 5.7, suggests that roughening of the SiO₂ film occurs on the surface of the Si MEMS substrate after cyclic actuation. The revealed surface roughening effect at stress concentrations during cyclic loading can be attributed to stress-assisted dissolution of the surface oxide layer, thereby, forming deep grooves in the vicinity of the notch that becomes sites for crack initiation. This is also shown to be consistent with the linear perturbation analysis that suggests that the evolution of surface topography is associated with stress-assisted dissolution of SiO₂ film.

5.4.2 Effects of Surface Oxide Thickening on Crack Driving Forces

To estimate the energy release rate from Equations (5.16), the coefficient (s) and the fitting parameter (λ) in Equation (5.17) are approximately equal to 0.425 and -0.0437, respectively, as obtained from Ref. 36. The material properties of SiO₂ film ($E = 72$ GPa and $\nu = 0.2228$ [29, 36]) and Si MEMS substrate ($E = 169$ GPa and $\nu = 0.22$ [37]) were used to compute energy release rates for two cases. First, the energy release rate ranges were evaluated as a function of oxide layer thicknesses for different cracks length in the topical SiO₂ layer and secondly, as a function of crack length for different thicknesses of the SiO₂ layer. The results of the energy release rate calculations are presented in Figures 5.8a and 5.8b, respectively.

From Figure 5.8a, it can be deduced that the thickness of the SiO₂ layer sets the size scale for the crack driving force, especially when the SiO₂ layer is greater than a certain thickness (~30 nm). This is consistent with the results of Shrotriya et al. [26, 29], where stable crack growth are predicted to occur in the topical SiO₂ layer when the crack driving force exceeds the crack growth threshold for stress corrosion cracking.

However, further thickening of the oxide layer leads ultimately to the SiO₂ fracture toughness being exceeded, when the oxide layer thickness exceeds the critical thickness of ~60 nm [29]. The above results (Figure 5.8a and 5.8b) are also consistent with those of Muhlstein et al. [21] in which oxide thickening and stress corrosion cracking has been reported in polysilicon MEMS structures with an oxide thickness of ~30-100 nm.

Since the maximum energy release rate for SiO₂ film with thickness below ~20 nm is less than the stress corrosion cracking threshold, stable subcritical crack growth in the polysilicon layer is unlikely until the topical oxide film thickness exceeds ~20 nm [29]. Similarly, the computed plots of energy release rate versus nominal crack length in Figure 5.8 suggest that the onset of fracture instability is unlikely to occur until the oxide thickness exceeds ~60 nm, as shown by Shrotriya et al. [29]. This again is consistent with the results of Muhlstein et al. [21] in which maximum oxide thicknesses of ~100nm were observed using high voltage TEM.

However, prior work by Alsem et al. [39] have shown experimentally the difference between thick (20 ± 5 nm) and thin (3.5 ± 1.0 nm) native oxide devices, but indicate that the difference in surface roughness may also be important. They showed that the thicker oxides and lower fracture strengths of the films resulted in an increased susceptibility of these films to cyclic fatigue failure, which they believed to have failed as a result of environmentally assisted subcritical cracking in a cyclic-stress assisted thickened silicon oxide.

Pierron and Muhlstein [40] also presented a numerical model that accounts for an alternative failure scenario where stable crack growth in the oxide changes to unstable crack growth when the crack hits the silicon/oxide interface. Their results indicated that polycrystalline silicon thin films are susceptible to fatigue failure when fracture strengths are higher than 5GPa and surface oxide layers thicker than 15 nm. The mechanism also

explained the decreasing growth rates observed for cracks propagating within the oxide layer; as these cracks approach the SiO₂/Si interface [40].

Furthermore, the associated energy release rate range is 10.3 J/m², for cracks that span 80% thickness of the oxide (Figure 5.8a). This is clearly greater than the fatigue threshold of 2 J/m² obtained for short cracks in Si MEMS thin films [29]. This is consistent with the results of Shrotriya et al. [26, 29], who pointed out that stable crack growth can occur in the SiO₂ layer when the energy release rate exceeds the stress corrosion cracking threshold [29]. From the above analysis, it is clear that the native oxide layer, with thicknesses on the order of a few nanometers, is enough to promote fatigue crack initiation, even after it thickened on average during cyclic actuation. However, with the combined effects of the surface roughening and local oxide thickening there is a high possibility for crack growth to occur within the oxide layer. In such cases, it is possible for cracks to grow and either penetrate into the substrate or extend along the interfaces between the oxide film and the Si substrate during fatigue [27]. This is because the resulting crack driving forces for cracks that extend fully across the topical oxide films are sufficient for the cracks to penetrate into the silicon substrate [27].

Furthermore, since the fracture toughness of the silicon is comparable to that of the SiO₂ layer, unstable crack growth in the SiO₂ layer is likely to result in unstable crack growth in the silicon substrate. The thickening of the topical oxide layer, therefore, plays a crucial role in enhancing the driving force for the nucleation and growth of cracks in silicon MEMS structures.

5.4.3 Crack Growth and Failure

Since the roughened oxide film is assumed to crack during loading if the strain along the surface exceeds the threshold strain [24, 26], the stretching of the MEMS substrate surface controls the rate of dissolution of the material. To examine the effect of the stress-

assisted dissolution on the possible formation and growth of cracks, finite element analysis (FEA) was performed using ABAQUS. Typical results obtained from the FEA are presented in 5.9a – 5.9d. The Figures show the magnified displacements of the MEMS structure corresponding to the regimes in which crack growth occur at the notch.

Figure 5.9a shows a detailed finite element calculation of the principal stress distribution near the notch tip for an initial crack length of 0.02 μm . It is clear that there is stress concentration on the crack tip edge due to the presence of a notch, which consequently, increases the strain along the surface the MEMS substrate. A similar effect, though to a higher degree, is observed at the crack tip edge of the crack lengths 0.04 μm , 0.06 μm and 0.08 μm as shown in Figures 5.9b, 5.9c and 5.9d respectively. Thus, depending on the crack lengths and the crack driving forces, it may be difficult for cracks inside the native oxide layer to further extend into the Si substrate and develop into a macro crack, even after the average thickness did increase during fatigue. However, if the increase in the crack driving force, with increasing crack length, drives the cracks to the full thickness of the films, (i.e. the cracks reach the film/substrate interface) then the cracks can either penetrate into the substrate or extend along the interfaces between the SiO_2 film and the Si MEMS substrate.

The results from the current study show that the former is most likely to occur, since there is no evidence of interfacial delamination observed in the SiO_2 film as the crack length increases (Figure 9a – 9d). Furthermore, final failure involved the fracture of the silicon substrate in all cases. There is, therefore, a potential to predict the total fatigue lives of silicon MEMS thin films by considering the combined effects of the crack growth in the oxide surface layers and the stress-assisted dissolution on the possible formation and growth of cracks.

5.5 Summary and Concluding Remarks

1) This paper explores the roles of stress-assisted dissolution and crack driving forces on the possible formation and growth of cracks in Si-MEMS structures. The cyclic actuation of Si-MEMS structures results in the thickening of surface SiO₂ films and the roughening of the surface oxide layer. The regions that are closer to the bottom of the notch of the actuated SiO₂ surface are found to have much higher surface roughness values (see Figure 6) due to the effects of stress-assisted dissolution of the topical SiO₂ layer.

2) As the surface of SiO₂ films roughens, the thickness of the SiO₂ layer sets the size scale for the crack driving force, especially when the SiO₂ layer is greater than a certain thickness (~30 nm). However, further thickening of the oxide layer leads ultimately to the SiO₂ fracture toughness being exceeded when the oxide layer thickness exceeds the critical thickness of ~60 nm. Hence, the increase in the crack driving force that occurs with increasing crack length drives the cracks to extend across the topical oxides until they penetrate into the silicon substrate to induce catastrophic failure/fracture.

3) Upon reaching the interfaces between the SiO₂ film and the Si MEMS substrate, the results from the finite element simulations suggest that final fracture is most likely to occur by fracture of the silicon substrate. Interfacial de-lamination (between the silicon substrate and the silica topical layer) is less likely to occur than substrate fracture, due to the relative magnitudes of the crack driving forces and substrate/interfacial fracture toughness values.

4) The results obtained from the perturbation analysis of stress-assisted surface dissolution are consistent with the measurements of surface topology evolution on polysilicon MEMS structure obtained by Shrotriya et al. [26, 29]. The perturbation analysis of the stress-assisted dissolution indicates that amplitudes of certain wave numbers will grow with time. This is consistent with plots of the Fourier transforms of the measured surface topology near the notch-tip before and after the actuation.

5) The results suggest that surface topography can evolve due to stress-assisted dissolution in the topical SiO₂ layer. However, such stress-assisted dissolution is unlikely to control the nucleation unless the oxide thicknesses are below ~20 nm. Instead, fatigue damage is likely to occur by stress corrosion cracking, when the surface oxide thickness is greater than ~20 nm. Also, since the crack driving force increases with increasing oxide thickness and crack length, unstable crack growth will initiate when the critical crack driving force for SiO₂ (~6 Jm⁻²) is reached. However, further work is needed to obtain the crack growth laws for the prediction of sub-critical crack growth in the topical silica layers under cyclic or static loading conditions.

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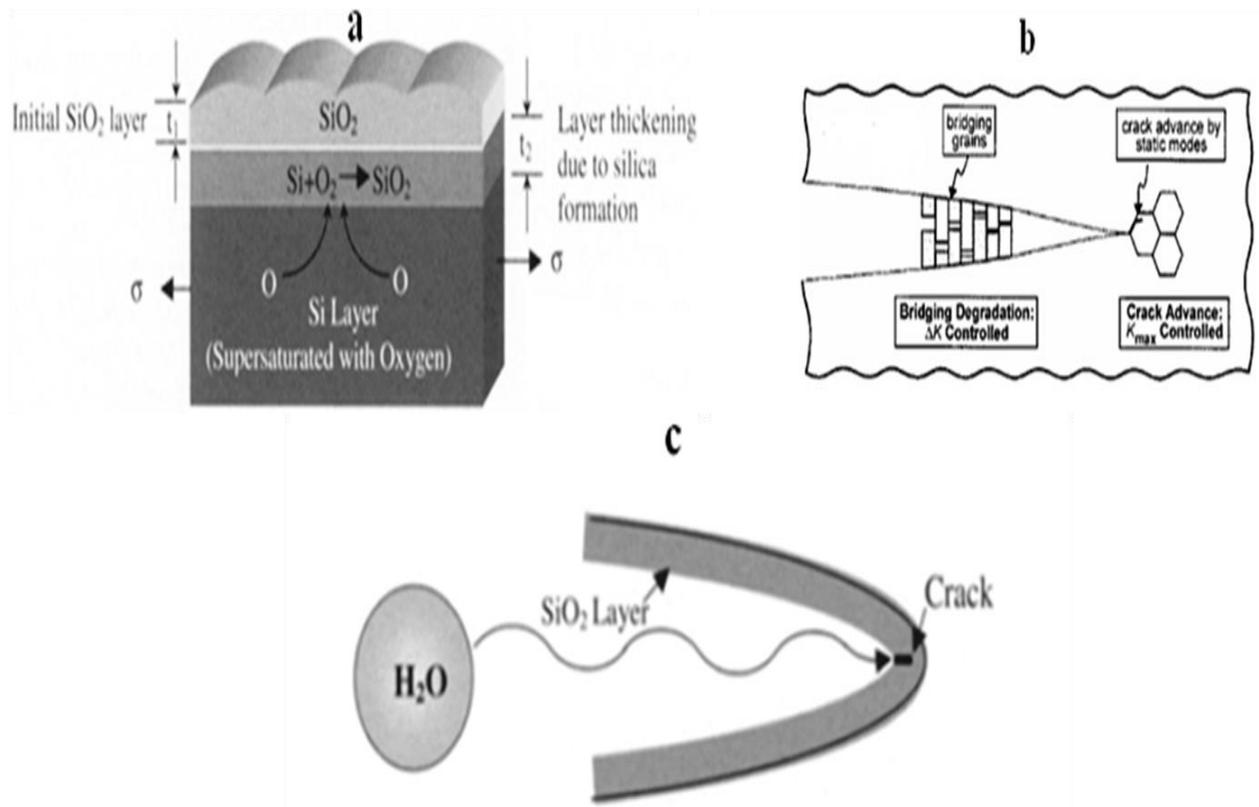


Figure 5.1: Proposed Mechanisms of Fatigue in Si MEMS Structures (a) Oxide Thickening Mechanism [29] (b) Mechanical Fatigue Mechanism [6] and (c) Slow Crack Growth Mechanism [29]

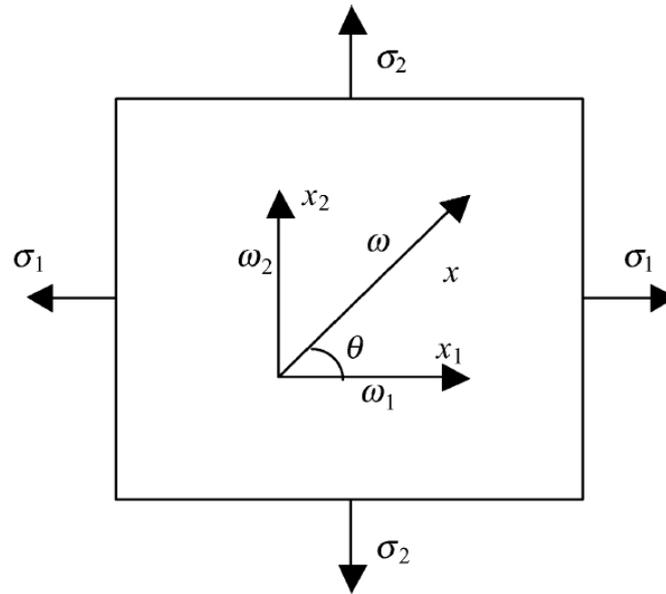


Figure 5.2: Geometrical conventions used in the model.

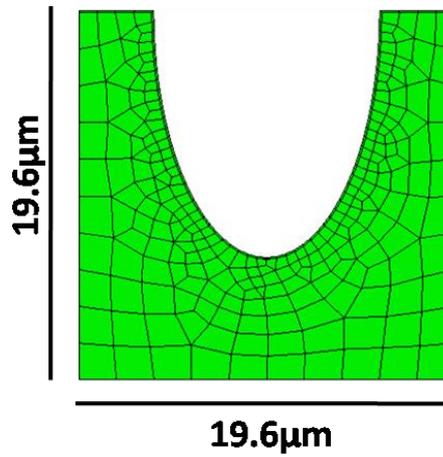


Figure 5.3: Geometry and mesh of the idealized structure for model.

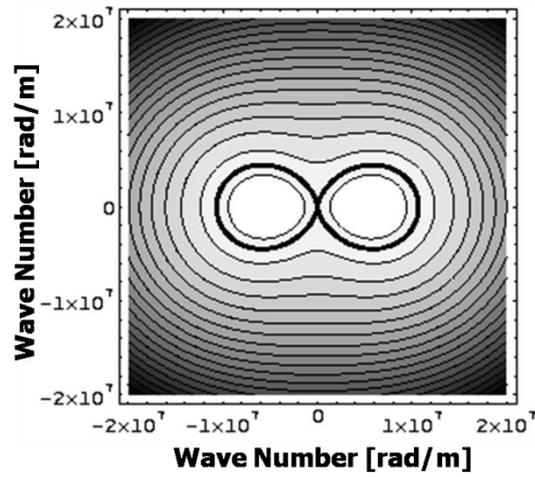


Figure 5.4: Contours of α corresponding to the stress state at the notch-tip.

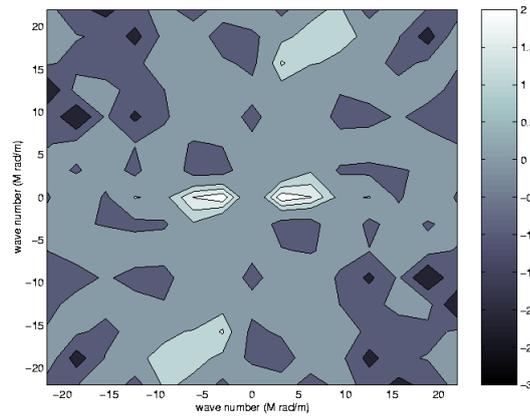


Figure 5.5: Contours of $\ln q(\omega, t)/q(\omega, 0)$ corresponding to an area of $2 \mu\text{m} \times 2 \mu\text{m}$ near the notch-tip. Taken from Ref. [26]

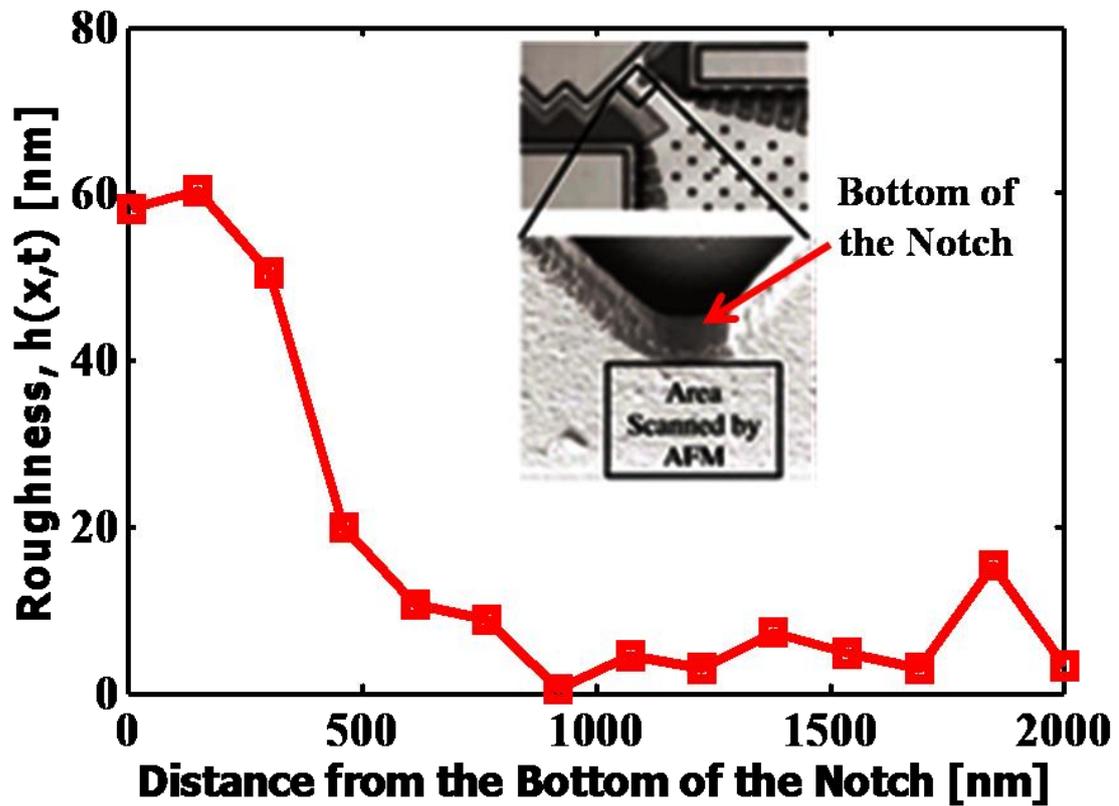


Figure 5.6: Computed surface roughness parameter $h(x, t)$ plotted against the distance from the bottom of the notch, insert: scanned AFM image, showing the bottom of the notch [24]

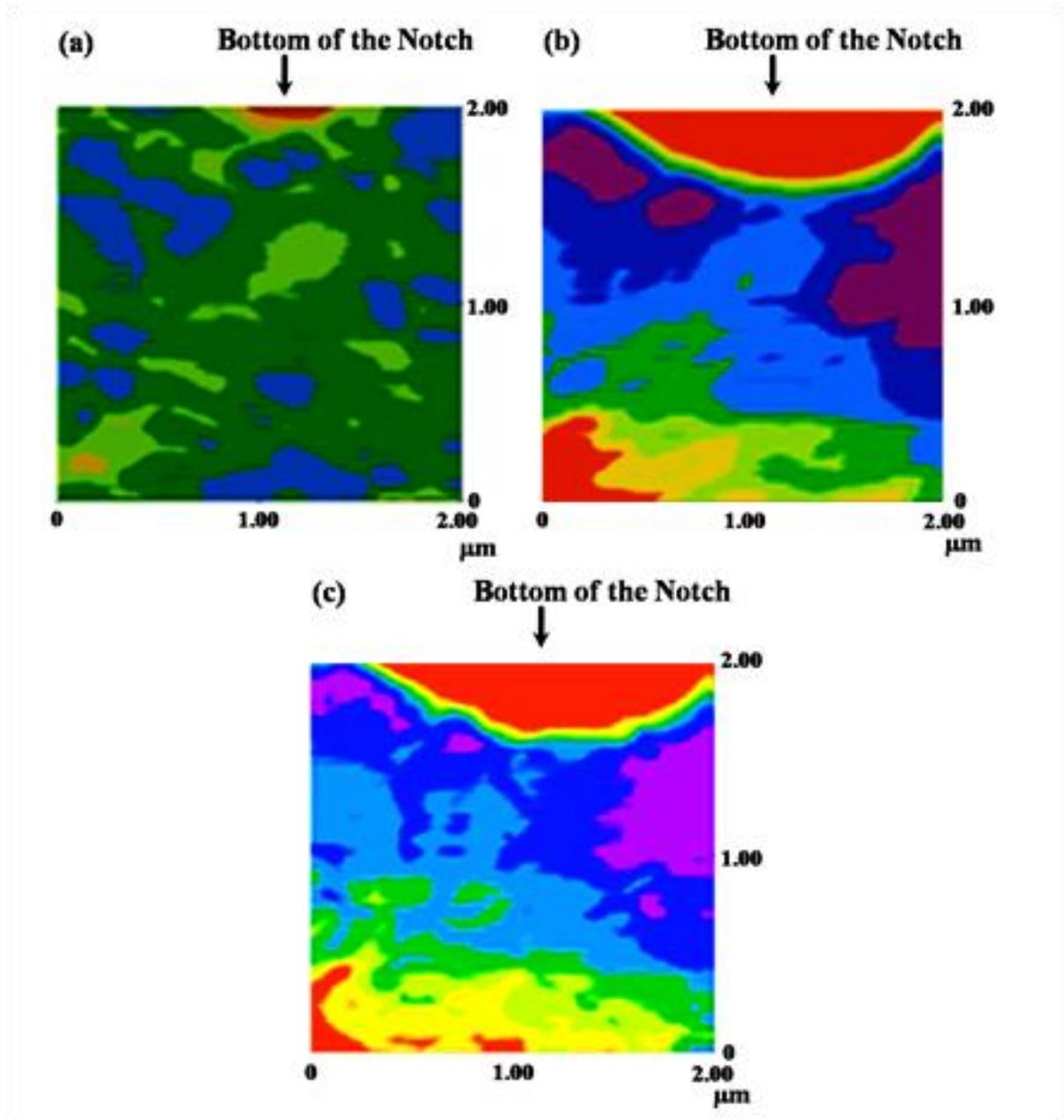


Figure 5.7: AFM quantitative depth analysis of the extent of change in the surface topography during actuation of polysilicon structures by image subtraction: (a) Before actuation, (b) After 12.79×10^9 cycles, and (c) Image subtraction. Take from Ref. [24].

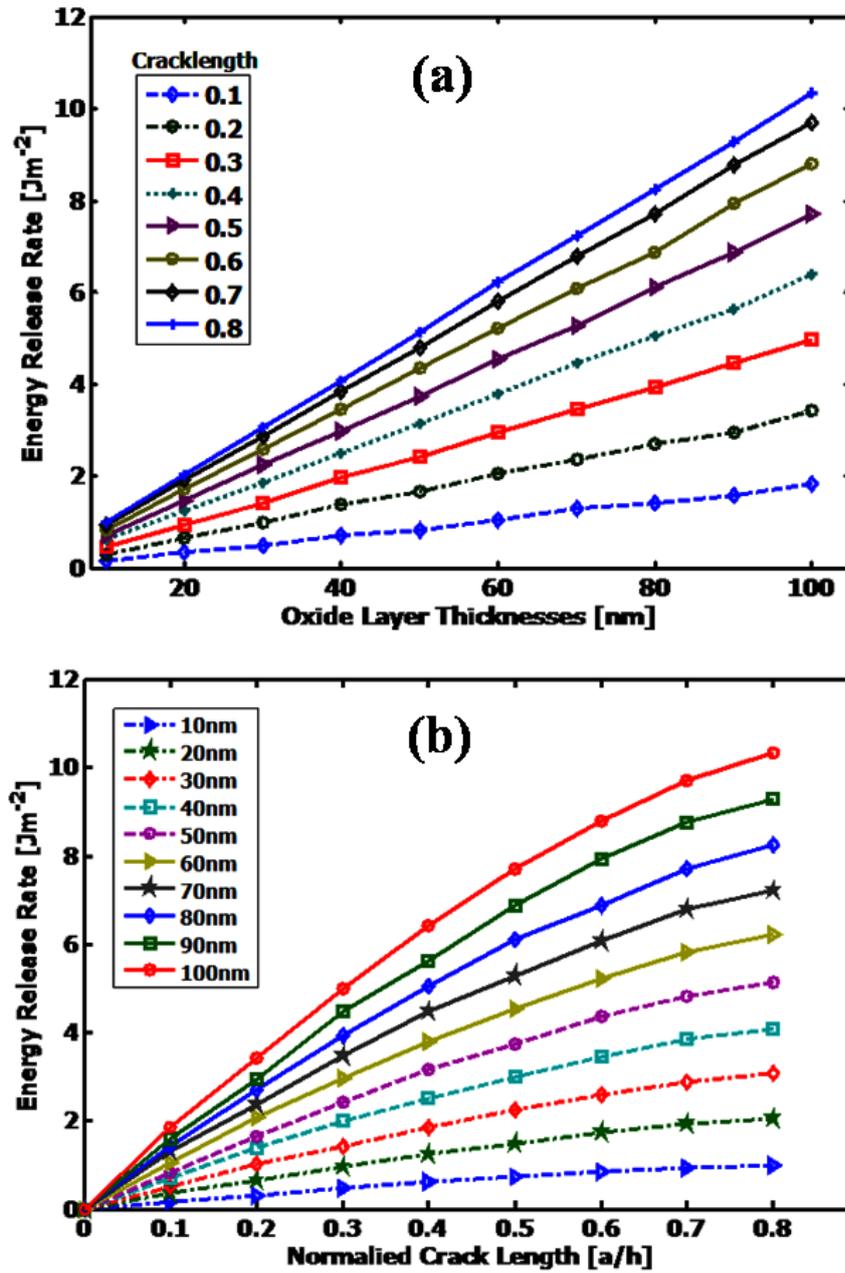


Figure 5.8: Energy release rates as a function of: (a) oxide layer thicknesses for different crack lengths in the topical SiO₂ layer, (b) crack lengths in the topical SiO₂ layer for different layer thicknesses

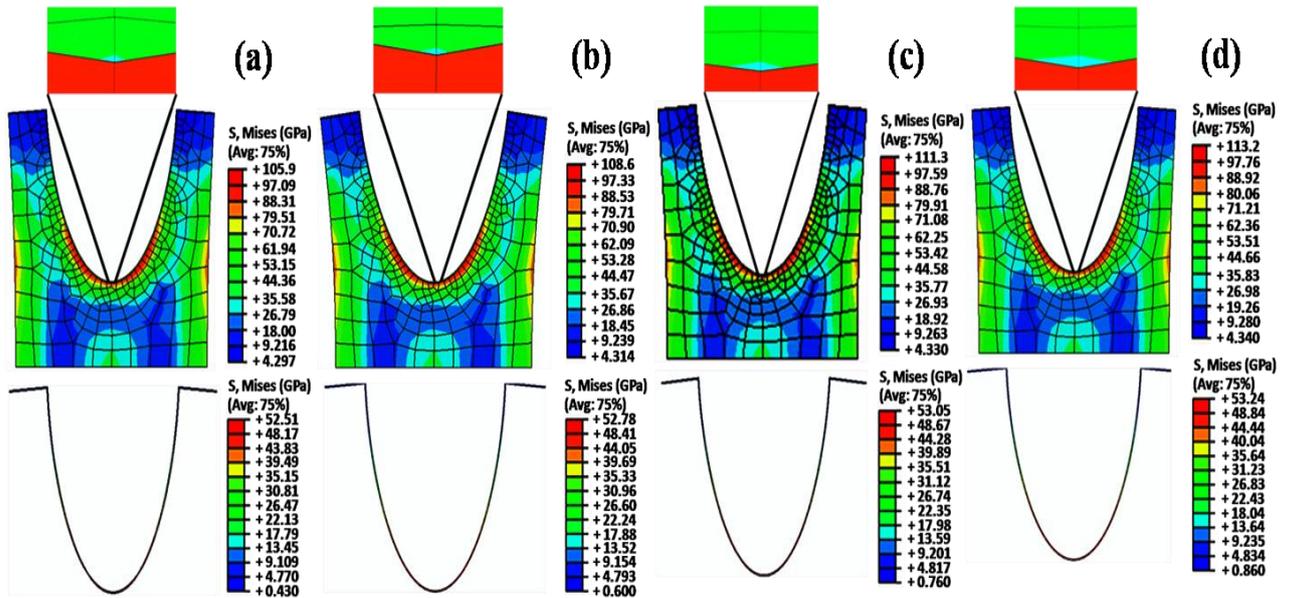


Figure 5.9: Finite element calculations: details of the principal stress distribution near the notch tip for crack length of (a) 0.02 nm, (b) 0.04 nm, (c) 0.06 nm, and (d) 0.08 nm.

CHAPTER SIX

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

This work has provided improved understanding of the effects of surface texture on the optical properties of silicon structures that are used for silicon solar cells and has also introduced a theoretical approach towards understanding the optical properties of texture silicon substrates at the micro- and macro-scales. It has also provided an improved understanding of the role of stress-assisted dissolution on the possible formation and growth of cracks in Si-MEMS structures. The salient conclusions arising from this study are summarized below:

6.1.1 Optical Reflectance of Alkali-Textured Silicon Wafers with Pyramidal Facets: 2D Analytical Model

In this section, a simple analytical model was developed to explore the optical behaviour of flat and textured silicon substrates for a full range of incidence angle to the silicon substrate. By characterizing the incident light and facets of the silicon wafer with vector geometry, dot products and Phong's reflection model were used to determine the reflection angles between incident light rays and pyramidal facets. The possible optical interactions are considered for a wide range of pyramidal geometries and light incidence angles that are relevant to the exposure of textured silicon surfaces to incident sunlight.

Furthermore, the model was used to investigate the possibility of secondary reflection, for the full range of incidence angles to the substrate. The reflectance predictions from the model were compared with measurements of reflectance on alkaline textured silicon surfaces. For all pyramid heights, it was found that the secondary reflection is guaranteed when the angle of incidence to the substrate is less than 19.4° . Consequently, any incident light beams

that strikes the textured surfaces of etched (001)-oriented silicon surfaces at low incidence angles, produces more secondary reflections than those with high incidence angles. As a result of this, secondary reflections increase the time available for the incident light rays to be absorbed into (001)-oriented silicon single crystals.

The predictions obtained in chapter three from the 2D textured surface model are close to the measured reflectance values presented in Literature. The close agreement between the experimental and predicted reflectance values suggests that the idealized model presented in chapter three captures most of the important aspects of light interactions with the pyramidal structures that are formed by the alkaline etching of (001)-oriented silicon surfaces with etchants such as KOH. These results demonstrate the significant of the model in the design of textured silicon surfaces for the control of surface reflectance and the trapping of light by secondary reflections. Such control and trapping could lead to increased photo-conversion and silicon solar cell efficiency.

6.1.2 Surface Texture and Optical Properties of Crystalline Silicon Substrates

In this chapter, the effects of KOH: IPA etching of (001)-oriented silicon single crystals was explored. The section presents the results of an experimental study of the effects of surface texture on the optical and light trapping properties of silicon wafers. Surface texture is controlled by anisotropic etching with potassium hydroxide (KOH) and isopropyl alcohol (IPA) solutions. The anisotropic etching of (001) crystalline silicon wafers is shown to result in the formation of {111} pyramidal facets on the surfaces of the wafers. A combination of profilometry, optical microscopy, scanning electron microscopy (SEM) and atomic force microscopy (AFM) is used to study the effects of KOH/IPA etching on the morphology and roughness of the textured surfaces. The results show that IPA concentration has the strongest effect on the surface roughness of (001)-single crystal crystals at temperatures up to 80°C.

The best volume concentration ratio of KOH: IPA is also found to be 2:4. For the durations and temperature ranges investigated in this study, the highest average surface roughness value of 676 nm was obtained for an etch time of 60 minutes at an etching temperature of 90⁰C. However, at higher etch temperatures, the dimensions of the pyramids increases. Hence, for example, the pyramids formed at 90⁰C are larger than those formed at 70⁰C. The etch rate also increases with increasing etching temperature/duration and increasing concentration of KOH. However, the volume concentrations of KOH: IPA above 2:4 can give rise to surface damage after exposures of ~ 1 hour. Increasing volume concentration of IPA also results in smoother pyramidal facets on (001)-oriented silicon surfaces.

The reductions in surface reflectance associated with controlled etching of (100)-oriented silicon wafers with KOH: IPA mixtures suggest that the controlled etching can be used to trap light by the formation of textured silicon surfaces that promote multiple reflections. The increased interactions with incident light rays can enhance the amount of light absorbed by (001) silicon single crystals. Thus, the optimization of KOH texturing process for silicon substrates provides an improved surface in terms of morphology and surface roughness thereby presenting same for use in solar cell application.

6.1.3 Modeling of Fatigue Failure in Silicon MEMS Structures

This study explored the role of stress-assisted dissolution on the possible formation and growth of cracks in Si-MEMS structures. This study presents the results of an analytical and computational model to study fatigue crack nucleation in Si-MEMS structures. To examine the effect of the stress-assisted dissolution on the possible formation and growth of cracks, finite element analysis was performed for topical SiO₂ layer on the silicon structures using ABAQUS FEM software. The possible evolution of thin layer is simulated and

compared with measured surface profiles from prior work. The possible formation and growth of cracks by such dissolution was elucidated.

The results show that the cyclic actuation of Si MEMS structures causes the thickening of surface SiO₂ films and the roughening of the surface film oxide. The regions that are closer to the bottom of the notch of the actuated SiO₂ surface are found to produce much higher surface roughness (see Figure 5.6). The similarities between the profiles obtained from theoretical predictions of the linear perturbation analysis and Fourier transform of the measured data indicate that topographical changes can only be attributed to effects of stress-assisted dissolution process.

Furthermore, it is clear from the analysis above that as the surface of SiO₂ films roughens, the thickness of the SiO₂ layer sets the size scale for the crack driving force, especially when the SiO₂ layer is greater than a certain thickness (~30 nm). Moreover, combining the effect of the surface roughening and local oxide thickening of the order of ~60-100 nanometers, there is high possibility that a crack within the oxide layer to grow within the oxide layer to grow and reach the interfaces between the SiO₂ film and the Si MEMS substrate.

However, the results from the finite element calculation suggest that final fracture is most likely to occur by fracture of the silicon substrate. Interfacial delamination (between the silicon substrate and the silica topical layer) is less likely to occur than substrate fracture, due to the relative magnitudes of the crack driving forces and substrate/interfacial fracture toughness values. Finally, the above results also suggest that the fatigue lives of silicon MEMS structures may be predicted using a combination of perturbation analyses and fracture mechanics models. However, further work is needed to obtain the crack growth laws for the prediction of sub-critical crack growth in the topical silica layers under cyclic or static loading conditions.

6.2 Future Work in this Research

6.2.1 Optical Reflectance of Alkali-Textured Silicon Wafers with Pyramidal Facets: 2D Analytical Model

Further work can be done to modify the 2D textured surface model developed in this study, by further exploring a 3D textured surface model. The 3D analytical model can consider the tertiary reflections to further obtained more accurate results. Meanwhile, a more realistic approach is needed to model the light/pyramid interactions in actual etched (001)-oriented silicon wafers with textures similar to those presented in Figure 3.1 and Figure 4.2. The approach cannot be achieved analytically and thus would require a ray tracing software.

6.2.2 Surface Texture and Optical Properties of Crystalline Silicon Substrates

A wide range of texturing parameters was investigated to further improve the understanding of the role of IPA in silicon surface texturing. While the effects of surface texture on the optical and light trapping properties of silicon wafers was explored in this study, solar cell devices should be further fabricated, both on flat and texture substrates to ascertain the absorption and device efficiency enhancement. Further work is clearly needed to explore the possible improvements in solar cell efficiency that can be achieved via the controlled alkaline etching of silicon wafers in silicon solar cells. Future research could also expand on these findings and determine the effect of etch depth on electrical properties of the c-Si solar cell devices.

6.2.3 Modeling of Fatigue Failure in Silicon MEMS Structures

Further work is needed to strengthen this section's results. First, the crack growth laws for the prediction of sub-critical crack growth in the topical silica layers under cyclic or static loading conditions needs to be obtained. Likewise, the oxide thickening mechanism is not yet well understood and further work is needed to address this issue or concern. Further research could also be done to improve the findings on the effect of stress-assisted dissolution process.